

II-YEAR ECE SYLLABUS-2022 SCHEME



Department of Electronics and Communication Engineering

GLOBAL ACADEMY OF TECHNOLOGY

(Autonomous institution affiliated to VTU, Belagavi. Accredited by NAAC with 'A' grade, NBA Accredited CS, E&C, E&E, MECH, CV and IS branches) Ideal Homes Township, Raja Rajeshwari Nagar, Bengaluru-560098.

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Global Academy of Technology, Bengaluru (Autonomous Institution Affiliated to VTU)

Scheme of Teaching and Examination 2022-23

Electronics and Communication Engineering

III SEMESTER -UG

SI.	Course	Course Title	Course Type	Teaching		eachii ırs/W		Ex	aminat	ion	CREDITS
No.	Code			Dept.	L	T	Р	CIE	SEE	Total	
1	22MAT31E	Transforms, Complex Variables and Special Functions	BS	MAT	2	2	0	50	50	100	3
2	22ECE32	Analog Electronic Circuits (Integrated)	IPC		3	0	2	50	50	100	4
3	22ECE33	Design and Analysis of Digital Circuits	PC	Respective	3	0	0	50	50	100	3
4	22ECE34	Network Analysis	PC	Department	2	2	0	50	50	100	3
5	22ECE35	Object Oriented Programming using C++	ESC/ETC/PLC		2	0	2	50	50	100	3
6	22ECE36	Sensors and Instrumentation	AEC		3	0	0	50	50	100	3
7	22ECEL37	Digital System Design Laboratory	PCL		0	0	2	50	50	100	1
						T	otal	300	300	700	20



Global Academy of Technology, Bengaluru (Autonomous Institution Affiliated to VTU)

Scheme of Teaching and Examination 2022-23

Electronics and Communication Engineering

IV :				

SI.	Course	Course Title	Course Type	Course Type Teaching		Teaching Hours/Week			Examination				
NO.	No. Code			Dept.	L	Т	Р	CIE	SEE	Total			
1	22MAT41E	Advanced Linear Algebra and Probability	BS	MAT	2	2	0	50	50	100	3		
2	22ECE42	Principles of Communication Systems (Integrated)	IPC		3	0	2	50	50	100	4		
3	22ECE43	Control Systems	PC	Respective	2	2	0	50	50	100	3		
4	22ECE44	Signals and Systems	PC	Department	2	2	0	50	50	100	3		
5	22ECE45	Data Structures using C++	ESC/ETC/PLC		2	0	2	50	50	100	3		
6	22ECE46	Verilog HDL	AEC		3	0	0	50	50	100	3		
7	22ECEL47	HDL Laboratory	PCL		0	0	2	50	50	100	1		
	Total 300 300 700 20												



SEMESTER - III

Course: Transforms, Complex Variables and Special Functions (For ECE)

Course Code	22MAT31E	CIE Marks	50
Hours/Week (L: T: P)	2:2:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: To enable students to apply the knowledge of Mathematics in various fields of engineering by making them to learn:

	0 01 0
CLO1	Laplace Transforms
CLO2	Fourier series of periodic functions
CLO3	Fourier Transforms
CLO4	Analytic functions and complex line integrals
CLO5	Bessel's and Legendre differential equations

Content	No. of Hours / RBT levels
Module 1 Laplace transforms of elementary functions, Laplace transforms of Periodic functions, unit-step function and Dirac delta function. Inverse Laplace Transform, Convolution theorem (without Proof), Solution of second order linear differential equations using Laplace transforms.	08 Hours L2, L3
Module 2 Fourier series of periodic functions, Complex form of Fourier series. Infinite Fourier transforms, Fourier sine and cosine transforms. Inverse Fourier transforms.	08 Hours L2, L3
Module 3 Function of a complex variable, Analytic Functions-Cauchy-Riemann equations in Cartesian and polar forms. Construction of analytic functions using Milne Thompson method. Properties of analytic functions.	08 Hours L2, L3
Module 4 Conformal Transformations, Bilinear transformations. Complex line integrals, Cauchy's theorem, Cauchy's integral formula. Singularities, poles, residues, Cauchy's residue theorem.	08 Hours L2, L3
Module 5 Series solution of Bessel's differential equation leading to Jn(x)-Bessel's function of first kind. Basic properties and orthogonality. Series solution of Legendre's differential equation leading to Pn(x)-Legendre Polynomials. Rodrigue's formula (without proof), problems.	08 Hours L2, L3

Course Outcomes: Upon completion of this course, student will be able to:

C Ou. 5C C	daise datedines. Open completion of this course, student will be usic to:							
CO31.1	Determine Laplace and inverse Laplace transforms of given functions leading to the							
CO31.1	solution of linear differential equations							
CO31.2	Apply Fourier series to transform periodic signals into fundamental frequencies							
CO31.3	Apply Fourier Transforms to transform continuous time signals from time domain to							
CU31.3	frequency domain and vice versa							
CO31.4	Apply Cauchy Riemann equations to study different properties of analytic functions							
CO31.5	Evaluate complex line integrals							
CO31.6	Apply the knowledge of Infinite Series to solve Bessel's and Legendre differential							
CU31.6	equations							



Textbooks:

- 1. B. S. Grewal, Higher Engineering Mathematics, Khanna Publishers 44th Edition, 2017
- 2. B.V. Ramana, Higher Engineering Mathematics, Tata McGraw-Hill, 2006

Reference Books:

- 1. E. Kreyszig, Advanced Engineering Mathematics, John Wiley & Sons 10th Edition, 2016
- 2. N.P.Bali and Manish Goyal, A Textbook of Engineering Mathematics, Laxmi Publications 6th Edition, 2014

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question from each module.**

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component and 10 marks would be exclusively for assignments. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs) and three tests. **Some possible AATs:** seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other.

Typical Evaluation pattern for regular courses is shown in Table 2.

Table 2: Distribution of weightage for CIE & SEE of Regular courses

	<u> </u>		
	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	Γ0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping															
CO/PO	PO1	PO2	P03	PO4	PO5	P06	PO7	P08	P09	PO10	PO11	PO12	PSO1	PSO2	PSO3	PS04
CO1	3	2	1									3				
CO2	3	2	1									3				
CO3	3	2	1									3				
CO4	3	2	1									3				
CO5	3	2	1									3				
CO6	3	2	1									3				
Average	3	2	1									3				

Low-1: Medium-2: High-3

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SEMESTER - III

Course: Analog Electronic Circuits (Integrated)

	•	· ·	
Course Code	22ECE32	CIE Marks	50
Hours/Week (L: T: P)	3:0:2	SEE Marks	50
No. of Credits	4	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Working, characteristics and biasing of FET
CLO2	JFET small signal model for various biasing circuits.
CLO3	Performance BJT Power amplifiers
CLO4	Applications of Operational Amplifiers and Wave form generators.
CLO5	Active filters and Data Converters.

Content	No. of Hours / RBT levels
Module 1	8 Hours
Field Effect Transistors: Introduction, Construction and Characteristics -	L3
of JFETs, Transfer Characteristics, Depletion type MOSFET, Enhancement	
type MOSFET and CMOS inverter.	
FET Biasing: Introduction, Fixed bias configuration, Self-bias	
configuration Voltage-Divider biasing.	
(Text-1:6.1, 6.2, 6.3, 6.7, 6.8, 6.11, 7.1, 7.2, 7.3 & 7.4)	
Module 2	8 Hours
FET Amplifiers: Introduction, JFET small signal model, Fixed- bias	L3
configuration, self-bias configuration (bypassed and unbypassed Rs)	
Voltage divider configuration, source follower, Low frequency response-	
FET amplifier, Miller effect capacitance, High frequency response- FET	
amplifier. (Text-1: 8.1, 8.2, 8.3, 8.4, 8.5, 8.7, 9.9, 9.10 & 9.12)	
Module 3	8 Hours
Power Amplifiers: Amplifier types, Series fed class A amplifier,	L3
Transformer coupled class A amplifier, Class B amplifier operation and	
Class B Amplifier Circuits-Transformer coupled push-pull circuit and	
Complementary-symmetry circuits, Amplifier distortion, Class C and Class	
D amplifiers. (Text-1: 12.1, 12.2, 12.3, 12.4, 12.5, 12.6 & 12.8)	
Module 4	8 Hours
Operation Amplifier Applications : Instrumentation amplifier, Op-Amp	L3
circuits using diodes-Half Wave Rectifier, Full Wave rectifier, Peak	
Detector, Clipper and Clamper, Sample and Hold circuit, Log and Antilog	
amplifier. (Text-2: 4.3, 4.6, 4.7 & 4,8)	
Comparators and Waveform Generators: Comparator- Non-inverting and	
inverting, Zero Crossing detector, Schmitt Trigger, Basic principles of sine	
wave oscillators-RC phase shift oscillators and Wien Bridge	
Oscillator.(Text-2: 5.2, 5.3 & 5.7)	
Module-5	8 Hours
Active Filters: Introduction, RC Active Filters- First order and Second order	L3
low pass filters, High pass Filter, Band-pass Filter, Band Rejection Filter.	
(Text 2: 7.1, 7.2- 7.2.1, 7.2.2, 7.2.4, 7.2.5 & 7.2.6)	



D-A and A-D Converters: Basic DAC Techniques- Weighted Resistor DAC, R-2R Ladder DAC, A-D converters: Parallel Comparator (Flash) A/D Converter, Successive Approximation Converter and DAC/ADC Specifications (Text 2: 11.2.1, 11.2.2, 11.3, 11.3.1, 11.3.4 &11.4)

	Practical Component of IPC					
	List of Experiments (use Hardware components and simulation tool)					
1	Conduct an experiment to draw the Drain and Transfer characteristics of MOSFET					
2	Simulate an experiment to draw the Drain and Transfer characteristics of JFET.					
3	Simulate Class-B push pull power amplifier and demonstrate its output waveform for					
	the given specific input.					
4	Design and Conduct Half wave and Full wave Precision Rectifier					
5	Design and conduct an experiment for Clippers using Op-Amp					
6	Design and conduct an experiment for Sample and Hold circuit using Op-Amp					
7	Design and Conduct Schmitt Trigger for given UTP and LTP					
8	Design and simulate First/ Second order active Low-Pass Filter (LPF) and High-Pass					
	Filter (HPF) for a given cut-off frequencies.					
9	Design and simulate RC phase shift oscillators using Op-Amp.					
10	Design and Conduct R-2R type Digital to Analog Converter.					

Course Outcomes: Upon completion of this course, student will be able to:

CO1	Explain operation and performance parameters of FET and MOSFET.
CO2	Analyze the performance of FET amplifiers
CO3	Evaluate the performance of Power Amplifiers
CO4	Describe the various applications of Operational Amplifiers
CO5	Analyze the different types of active filters, Data Converters.

Textbooks:

- 1. Robert L. Boylestad and Louis Nashelsky, Electronics devices and Circuit theory, 10/11thEdition, Pearson, 2021
- 2. D Roy Choudhury and Shail B Jain, Linear Integrated Circuits, 5th Edition, New age International Limited, 2015.

Reference Books:

- 1. J. Millman and C. C. Halkias, Integrated Electronics, 2nd Edition, Tata Mc-Graw Hill Publishing Company Limited, 2017
- 2. Behzad Razavi, Fundamentals of Microelectronics, John Weily, 2013

E-Books / Web References:

- 1. http://www.springer.com/engineering/electronics/book/978-0-387-25746-4,Analog Circuit Design: A Tutorial Guide to Applications and solutions.
- 2. https://www.tutorialspoint.com/linear integrated circuits applications/index.htm
- 3. https://www.scribd.com/book/282535091/Linear-Integrated-Circuits

MOOCs:

https://nptel.ac.in/courses/108/106/108106084/https://nptel.ac.in/courses/108/102/108102095/https://nptel.ac.in/courses/117/103/117103063/https://www.khanacademy.org/



Scheme of Examination: (Integrated courses)

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question from each module.**

The laboratory assessment of Integrated courses would be restricted to only the CIE evaluation.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. The average of the three tests are taken for computation of CIE on a scale of 30 and CIE would also include laboratory evaluation for 20 marks. The laboratory marks of 20 would comprise of 10 marks for regular laboratory assessment to include lab record and observation and 10 marks would be exclusive for laboratory internal assessment test to be conducted at the end of the semester. The Evaluation pattern for integrated courses is shown in the Table-1

Table-1: Distribution of weightage for CIE & SEE of Integrated courses

	Component	Marks	Total Marks
	CIE Test-1	30	
CIE	CIE Test-2	30	F0
CIE	CIE Test-3	30	50
	Laboratory	20	
SEE	Semester End Examination	100	50
		Grand Total	100

					CC	D-PO a	nd PS0	O map	ping					
СО	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	1	-	-	-	-	-	-	-	-	2	1
CO2	3	2	2	1	-	-	-	-	-	-	1	-	2	1
CO3	2	1	-	ı	-	-	-	-	-	-	1	-	1	-
CO4	3	2	2	1	-	-	-	-	-	-	-	1	2	1
CO5	3	2	2	1	-	-	-	-	-	-	1	1	2	1
Average	3	2	2	1	-	-	-	-	_	_	_	1	2	1

Low-1: Medium-2: High-3



SEMESTER – III

Course: Design and Analysis of Digital Circuits

Subject Code	22ECE33	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Concepts of simplifying Boolean expression using K-map techniques and Quine Mc
	Cluskey minimization techniques.
CLO2	Adders, Subtractors, Encoders, Decoders, Multiplexers and Comparators.
CLO3	Methods and analysis of sequential logic circuits.
CLO4	State diagrams of synchronous sequential circuits.
CLO5	PLDs, and Hazards in Combinational Networks.

Contont	No. of Hours / RBT levels
Module 1	8 Hours
Principles of Combinational Logic: Definition of combinational logic, Canonical	L3
forms, Generation of switching equations from truth tables, Karnaugh maps-up	
to 4 variables, Quine-Mc Cluskey Minimization Technique. (Text 1:3.1, 3.2, 3.3, 3.4 & 3.5)	
Module 2	8 Hours
Logic Design with MSI Components: Binary Adders and Subtractors, Decimal	L3
Adders, Comparators, Decoders, Encoders, and Multiplexers. (Text 2: 5.1.1, 5.1.2, 5.2, 5.3, 5.4, 5.5 & 5.6)	
Module 3	8 Hours
Flip-Flops and their Applications: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip-flops, Characteristic equations, Registers, Counters, Design of Synchronous mod-n Counter using clocked T, JK, D, and SR flip-flops. (Text 2: 6.4.1, 6.4.2, 6.6, 6.7, 6.8, 6.9.1 & 6.9.2)	L3
Module 4	8 Hours
Sequential Circuits Design and Analysis II: Mealy and Moore Models, State Machine notation, Synchronous Sequential Circuit Analysis. Construction of State Diagrams, and Counter design. (Text 1:6.1, 6.2, 6.3, 6.4 & 6.5)	L3
Module 5	8 Hours
Programmable Logic Devices & Hazards in Combinational Networks: Programmable Logic Devices, Programmable Read-only Memories, Programmable Logic Arrays, Programmable Array Logic, Static and Dynamic Hazards in Combinational networks, Essential Hazards. (Text-2:5.7, 5.8, 5.9, 5.10, 9.9 & 9.10)	L3



Course Outcomes: After studying this course, students will be able to;

CO1	Simplify Boolean functions using K-map and Quine-McCluskey minimization
	techniques.
CO2	Analyze and design of Combinational logic circuits.
CO3	Explain the operation of Flip Flops (SR, D, T, and JK) and design the synchronous
	sequential circuits using Flip Flops.
CO4	Design and develop Mealy & Moore models and state diagrams of synchronous
	sequential circuits.
CO5	Describe various types of PLDs and Hazards in Combinational Networks.

Textbooks:

- 1. John M Yarbrough, Digital Logic Applications and Design, Thomson Learning, 2001.
- 2. Donald D. Givone, Digital Principles, and Design, Tata McGraw Hill Education, 2002.

Reference Books:

- 1. Charles H Roth Jr. Fundamentals of Logic Design, Cengage Learning,
- 2. Sudhakar Samuel, Logic Design, Pearson/ Sanguine, 2007.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminars/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. The Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks				
	CIE Test-1						
CIE	CIE Test-2	40	F0				
CIE	CIE Test-3	40	50				
	Assignments	10					
SEE	Semester End Examination	50	50				
	Grand Total						

	CO- PO and PSO Mapping													
COs	PO1	PO2	PO3	PO4	PO5	1	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	-	-	-	-	-	-	-	-	-	-	2	1
CO2	2	2	1	-	-	-	-	-	-	-	-	-	2	2
CO3	2	2	1	-	-	-	-	-	-	-	-	-	2	2
CO4	2	2	2										2	
CO5	2	2	2											
Average	2	2	2										2	2

Low-1: Medium-2: High-3

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SEMESTER - III

Course: Network Analysis

Course Code	22ECE34	CIE Marks	50
Hours/Week (L: T: P)	2:2:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Kirchhoff's Law and Laplace Transforms **Course Learning Objectives**: Students will be taught;

	0 ,
CLO1	Mesh and Nodal techniques to solve electrical networks.
CLO2	Concept of Network theorems to solve the electrical networks.
CLO3	Network parameters for two port networks.
CLO4	Transient behavior of electrical circuit during switching.
CLO5	Graphical method to solve electrical networks.

Content	No. of Hours/ RBT levels
Module 1	8 Hours
Basic circuit analysis concepts: Practical Sources, Source transformation,	L3
Star-Delta Conversion, Mesh analysis and Node analysis with dependent and	
independent sources for DC and AC networks. Concepts of super node and	
super mesh. (Text2)	
Module 2	8 Hours
Network Theorems: Superposition theorem, Thevenin's theorem, Norton's	L3
theorem, Maximum power transfer theorem, Reciprocity theorem and	
Millmans theorem. (Text2)	
Module 3	8 Hours
Two port Network Parameters: Definition of Z, Y, h and Transmission	L3
parameters, Modeling with these parameters and relationship between	
parameters. (Text2)	
Module 4	8 Hours
Transient behaviour and initial conditions: Behaviour of circuit elements	
under switching condition and their representation of initial and final	L3
conditions in RL, RC and RLC circuits for DC excitations, Application of Laplace	
for RLC Circuits. (Text3)	
Module 5	8 Hours
Graph Theory and Network equations : Graph of a network, Trees, Co-trees	L3
and Loops, Incidence Matrix, Cut-set Matrix, Tie-set Matrix and loop currents,	
Number of possible trees of a graph and Duality. (Text1)	

Course Outcomes: Upon completion of this course, student will be able to:

	Catedines. open completion of this course, student will be usic to.
CO1	Determine the current and/or voltage by simplifying an electrical network using mesh
	and node analysis.
CO2	Solve the electrical networks by applying theorems to reduce circuit complexities.
CO3	Determine Z, Y, h and T parameters and their inter relationship for a given two port
	networks.
CO4	Analyze the initial behaviour of the electrical circuit and find the network solution
	using Laplace transform
CO5	Estimate the current and/or voltage for the given electrical networks using Graph
	theory.

Textbooks:

- 1. D. Roy Choudhury, Networks and Systems, 2nd Edition, New Age International Pvt Ltd, 2010.
- 2. Ravish R. Singh, Electrical Networks, Tata McGraw-Hill Education, 2009.
- 3. VanValkenburg M. E. Network Analysis, 3rd Edition, Prentice Hall of India Pvt Ltd, 2002.

Reference Books:

- 1. Mahmood Nahvi, Joseph A. Edminister. Schaum's Outline of Electric Circuits, 6th Edition, McGraw-Hill Education, 2014.
- 2. Hayt, Kemmerly and Durbin, Engineering Circuit Analysis, 6th Edition, Tata McGraw-Hill Education, 2002.

MOOCs:

https://nptel.ac.in/courses/108/105/108105159/

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. The Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PSO1	PS02
CO1	3	3	1	-	-	-	-	-	-	-	-	1	2	-
CO2	2	3	2	1	-	-	-	ı	-	-	-	1	2	-
CO3	3	3	2	-	-	-	-	1	-	-	-	1	2	-
CO4	3	3	2	1	-	-	-	ı	-	-	-	1	2	-
CO5	3	3	2	1	_	-	-		-	-	-	1	2	-
Average	3	3	2	-	-	-	-	-	-	-	-	1	2	-

Low-1: Medium-2: High-3

SEMESTER – III

Course: Object Oriented Programming using C++

Course Code	22ECE35	CIE Marks	50
Hours/Week (L: T: P)	2:0:2	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Features of object-oriented programing.
CLO2	Data abstraction and encapsulation.
CLO3	Constructors, destructors and operator overloading.
CLO4	Inheritance and virtual functions.
CLO5	Templates and exception handling.

Content	No. of Hours / RBT levels
Module 1	8 Hours
Beginning with C++ and its features: What is C++?, Applications and	L2
structure of C++ program, Different Data types, variables, Different	
Operators, expressions, operator overloading and control structures in C++.	
(Text 1: 2.1-2.3, 3.1-3.24)	
Module 2	8 Hours
Functions, classes and Objects: Functions, Inline function, function overloading, friend and virtual functions, specifying a class, C++ program with a class, arrays within a class, memory allocation to objects, array of objects, members, pointers to members and member functions. (Text 1: 4.1 - 4.11, 5.3-5.5, 5.9, 5.10, 5.13-5.15 & 5.18)	L3
Module 3	8 Hours
Constructors and Destructors: Constructors, parameterized constructors, Multiple constructors in a class, Copy constructor, Dynamic constructor,	L3
Destructors.	
Operator overloading: Defining operator overloading, Overloading Unary	
and binary operators, Overloading Binary operators Using Friends, rules for	
overloading operators. (Text 1: 6.1-6.8, 7.1 - 7.5,7.8)	
Module 4	8 Hours
Inheritance and Polymorphism: Derived Classes, Single, multilevel, multiple	L3
inheritance, Pointers to objects and derived classes, this pointer, Virtual and	
pure virtual functions. (Text 1: 8.2-8.6, 9.3 -9.8)	
Module 5	8 Hours
Templates: Class Templates, class templates with multiple parameters,	L2
Function Templates, Function templates with multiple parameters,	
overloading of template functions, member function templates.	
Exception Handling : Basics of Exception handling, Exception handling	
Mechanism, Throwing an Exception, Catching an exception, Rethrowing an	
exception, Specifying Exceptions. (Text 1: 12.2-12.7, 13.2 – 13.7)	

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Course Outcomes: Upon completion of this course, student will be able to:

CO1	Describe the basic concepts of object-oriented programming language.
CO2	Implement the classes and objects using functions.
CO3	Explain constructors and destructors and develop programs to overload operators.
CO4	Develop programs by using inheritance and polymorphism.
CO5	Develop programs by using templates and exception handling mechanisms in C++.

Textbooks:

1. E. Balaguruswamy, Object Oriented Programming with C++, 7th Edition, Tata McGraw Hill, 2018.

Reference Books:

- 1. Robert Lafore, Object Oriented Programming using C++, 4th Edition, Galgotia publication, 2010
- 2. Herbert Schildt, C++ The Complete Reference, 4th Edition, McGraw Hill Education, 2017.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks			
	CIE Test-1	40				
CIE	CIE Test-2	40	F0			
CIE	CIE Test-3	40	50			
	Assignments	10				
SEE	Semester End Examination	50	50			
	Grand Total					

					CC	D-PO a	nd PS0) Мар	ping					
СО	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	1	1	1	-	1	-	1
CO2	3	2	-	-	-	-	-	1	1	1	-	1	-	1
CO3	3	2	-	-	-	-	-	1	1	1	1	1	1	1
CO4	3	2	-	-	-	-	-	1	1	1	-	1	-	1
CO5	3	2	-	-	-	-	-	1	1	1	-	1	-	1
Average	3	2	-	-	-	-	-	1	1	1	-	1	-	1

Low-1: Medium-2: High-3

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SEMESTER - III

Course: Sensors and Instrumentation

Course Code	22ECE36	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Concepts of Sensors and its classification.
CLO2	Self-Generating and Digital and Intelligent Sensors.
CLO3	Concepts of Measurement and Working of Digital Voltmeter and Instruments
CLO4	Measurement of various parameters using Bridges.
CLO5	Operations of Oscilloscopes, Signal Generators and Wave Analyzers.

Content	No. of Hours / RBT levels
Module 1	8 Hours
Introduction to sensor-based measurement systems: General concepts and terminology, Sensor classification, Primary Sensors-Temperature sensors, Pressure Sensors, Level sensors, Resistive Sensors-Potentiometer, Strain Gauge, Resistive Temperature detector, Thermistors. (Text 1: 1.1, 1.2, 1.7, 2.1, 2.2.1, 2.3 & 2.4.1)	L2
Module 2	
Self-generating Sensors: Thermoelectric sensors, Piezoelectric sensors, Pyroelectric sensors, Photovoltaic sensors, electrochemical sensors. Digital and Intelligent Sensors: Resonant Sensors- Sensor based on Quartz resonators, Digital Quartz Thermometer, Frequency Measurement, Period and Time Interval Measurement. (Text 1: 6.1.1, 6.2.1, 6.2.2, 6.3.1, 6.4.1, 6.5, 8.2.1, 8.2.1.1, 8.5.1 & 8.5.2)	8 Hours L2
Module 3	
Principles of Measurement: Static Characteristics, Error in Measurement, Types of Static Error, Source of Error. Digital Voltmeter: Introduction, Ramp Technique, Dual slope, integrating Type DVM, and Successive Approximations type DVM. Digital Instruments: Digital tachometer, Digital pH meter, Digital phase meter. (Text 2: 1.3, 1.4, 1.5, 1.6, 5.1, 5.2, 5.3, 5.4, 5.6, 6.9, 6.10 & 6.12)	8 Hours L3
Module 4	
Bridges: Wheatstone's Bridge, Kelvin's Bridge, AC Bridges – Capacitance Comparison bridge, Inductance Comparison bridge, Maxwell's Bridge, Wien's bridge. (Text2: 11.2, 11.2.1, 11.2.2, 11.2.3, 11.2.4, 11.2.5, 11.3, 11.8, 11.9, 11.10, 11.11 & 11.14)	8 Hours L3
Module 5	
Oscilloscopes: Introduction, Basic Principle, CRT Features, Block diagram of oscilloscope, Dual beam CRO, Dual Trace oscilloscope, Storage oscilloscope, Signal Generators: Standard Signal Generator, Function Generator, Random Noise Generator.	8 Hours L2

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Wave Analyzers: Basic wave analyzer, heterodyne wave analyzer, Spectrum Analyzer.

(Text 2: 7.1, 7.2, 7.3, 7.4, 7.14,7.15, 7.18, 8.5, 8.8, 8.10, 9.2, 9.4 & 9.6)

COURSE OUTCOMES: Upon completion of this course, student will be able to:

CO1	Understand the concept of Sensors and operation of primary sensors.
CO2	Describe the operation of various self-generating Digital and Intelligent Sensors.
CO3	Explain the operation of measurements and the operation of Digital voltmeter and
	Instruments.
CO4	Evaluate various measurement parameters using various bridges.
CO5	Elaborate the working of Oscilloscopes, Signal Generators and Wave Analyzers.

Textbooks:

- 1. Sensors and Signal Conditioning, Ramon Pallas Areny, John G. Webster, 2nd edition, John Wiley, and Sons, 2000
- 2. Electronic Instrumentation, H S Kalsi, Mc Graw Hill, 3rd edition, 2012

Reference book:

- 1. Electronic Instrumentation & Measurements, David Bell, Oxford University Press PHI, 2nd Edition, 2006.
- 2. Modern Electronic Instrumentation and Measuring Techniques, D. Helfrick and W.D. Cooper Pearson, 1stEdition, 2015.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any five full questions choosing at least one full question from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1.

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
CIE	CIE Test-1	40	
	CIE Test-2	40	50
CIE	CIE Test-3	40	- 50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		



	CO-PO and PSO Mapping													
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	-	-	-	-	-	-	-	-	-	-	1	-
CO2	1	1	1	-	-	-	-	-	-	-	-	-	1	1
CO3	1	2	-	-	-	-	-	-	-	-	-	1	1	-
CO4	3	3	2	-	-	-	-	1	-	-	-	1	2	1
CO5	2	1	-	-	-	-	-	1	-	-	-	1	2	1
Average	2	2	-	-	-	-	-	1	-	-	-	1	2	1

Low-1: Medium-2: High-3



SEMESTER -III

Course: Digital System Design Laboratory

Subject Code	22ECEL37	CIE Marks	50
Hours/Week (L: T: P)	0:0:2	SEE Marks	50
Credits	1	Examination Hours	03

Course Objectives: Students will be taught;

CLO1	Implementation of Boolean Expressions using Logic Gates.
CLO2	Implementation of various Combinational circuits.
CLO3	Implementation of various sequential circuits.
CLO4	Design of flip-flops and shift registers.
CLO5	Design of counters.

SI. No.	Experiments	RBT levels
	List of Experiments to be conducted using Hardware components/ Multisim/ PSpice	
1.	Realization of Boolean Expressions using logic gates.	L2, L3
2.	Realization of Binary Adder and Subtractor using Universal Gates.	L2, L3
3.	Implementation of Boolean functions using IC 74153 and IC 74139.	L2, L3
4.	Conversion of Binary to Gray Code and Vice-Versa using Ex-OR gates.	L2, L3
5.	Design a 2-bit Magnitude Comparator using logic gates and a 4-bit comparator using IC 7485.	L2, L3
6.	Verification of truth tables of Master-Slave JK, T, and D flip-flops using NAND gates.	L2, L3
7.	Verify the following operations using IC 7495 i) SISO (ii) SIPO (iii) PISO (iv) PIPO	L2, L3
8.	Design and verify the Johnson and Ring counter using IC 7495.	L2, L3
9.	a. Realize Asynchronous Mod–N counter using IC-7490, IC-74193, b. Realize Synchronous 3-bit UP/DOWN counter using IC 7476.	L2, L3
10.	Use simulation tool for the realization of Binary Adder and Subtractor using IC 7483.	L2, L3
11.	Use a simulation tool to verify the truth table of Master-Slave JK, T, and D flip-flops using NAND gates.	L2, L3
12.	Use a simulation tool for the realization of Asynchronous Mod –N counter using IC, 7490, IC 74193.	L2, L3

Course Outcomes: Upon completion of this course, student will be able to:

CO1	Illustrate the simplification of Boolean Expressions using Logic Gates.
CO2	Design of Binary Adders, Subtractors, and Comparators.
CO3	Implement the various Boolean functions.
CO4	Construct various types of flipflops and shift registers
CO5	Design and Realize the counters.



Textbooks:

1. Donald D. Givone, Digital Principles, and Design, Tata Mc-Graw Hill Publishing Company Limited, 2016.

Reference Books:

- 1. John M Yarbrough, Digital Logic Applications and Design, Cengage Learning, 2016.
- 2. M. Morris Mano, Digital Logic and Computer Design, Prentice Hall of India Publication, 2000.

MOOCs:

- 1. https://www.edx.org/course/digital-design-2
- 2. https://www.coursera.org/learn/digital-systems
- 3. https://onlinecourses.nptel.ac.in/noc19_ee51/preview

Scheme of Examination:

Semester End Examination (SEE):

All laboratory experiments are to be included for practical examination. Students can pick one experiment from the questions lot prepared by the examiners. Change of experiment is allowed only once and 15% Marks allotted to the write up part to be made zero.

Semester End Examination Evaluation			
SL.NO	ACTIVITY	MARKS	
1	Write-Up	15	
2	Conduction	70	
3	Viva Voce	15	
	TOTAL	100	

Note: The marks scored will be proportionately reduced to 50

Continuous Internal Evaluation (CIE):

As part of CIE process, progressive continuous evaluation is done for laboratory work on weekly basis of conduct of experiment by student either individually or in group based on the laboratory. The breakup of the marks allocated is given in the TABLE-1

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TABLE-1 WEEKLY EVALUATION OF CONDUCT OF EXPERIMENT				
SL.NO	ACTIVITY	MAX MARKS		
1	Conduct of experiment and documentation	10		
2	Analysis & interpretation of results	5		
3	Viva voce	5		
	TOTAL			

Internal examination is conducted at the end of the semester or on completion of a predefined set of experiments based on the laboratory. The evaluation detail of the laboratory internal exam is given in TABLE-2

TABLE-2 LAB INTERNAL EXAMINATION			
SL.NO	ACTIVITY	MAX MARKS	
1	Detailed write-up about the experiment with relevant procedure	5	
	and calculation.		
2	Conduction of experiment	20	
3	Viva voce	5	
	30		



	TABLE-3 FINAL CIE CALCULATION				
SL.NO	METRICS USED	MAX MARKS			
1	Average of all weekly evaluations of conduct of an experiment	20			
2	Lab Internal Examination	30			
	TOTAL				

	CO-PO and PSO Mapping													
CO/PO	PO1	P02	PO3	PO4	PO5	P06	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	1	-	-	-	-	-	1	-	-	-	2	-
CO2	2	2	1	-	-	-	-	-	1	-	-	-	2	-
CO3	2	2	1	-	-	-	-	-	1	-	-	-	2	-
CO4	2	2	1	-	2	-	-	-	1	-	-	-	2	-
CO5	2	2	1	-	2	-	-	-	-	-	-	-	2	-
Average	2	2	1	-	2	ı	ı	-	1	-	ı	ı	2	-

Low-1: Medium-2: High-3

SEMESTER -IV

Course: Advanced Linear Algebra and Probability (For ECE)

Course Code	22MAT41E	CIE Marks	50
Hours/Week (L: T: P)	2:2:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: To enable students to apply the knowledge of Mathematics in various fields of engineering by making them to learn:

CLO1	Probability distributions
CLO2	Stochastic process and Markov chains
CLO3	Sampling distributions and testing of hypothesis
CLO4	Linear Transformation
CLO5	Singular value decomposition

Content	No. of Hours/ RBT levels
Module 1 Probability, Axioms of probability, Conditional probability, Bayes theorem, Discrete and continuous random variables, Moments, Moment generating functions, Binomial, Exponential, Poisson, Normal distributions.	08 Hours L2, L3
Module 2	
Joint distributions of two discrete random variables, Marginal and conditional distributions, Expectation and Covariance. Stochastic processes, probability vector, stochastic matrices, fixed points, regular stochastic matrices, Markov chains, higher transition probability-problems.	08 Hours L2, L3
Module 3	
Sampling, Sampling distributions, standard error, test of hypothesis for means and proportions, student's t-distribution, chi-square distribution as a test of goodness of fit, F Test.	08 Hours L2, L3
Module 4	
Linear transformations, algebra of transformations, representation of transformations by matrices, linear functional, Non-singular Linear transformations, inverse of a linear transformation, Problems on Rank-Nullity theorem.	08 Hours L2, L3
Module 5	00 Hours
Eigen values and Eigenvectors, Diagonalization, quadratic Forms, constrained optimization, Singular value decomposition.	08 Hours L2, L3

Course Outcomes: Upon completion of this course, student will be able to:

CO41.1	Solve problems associated with random variables using probability distributions
CO41.2	Solve problems related to testing of hypothesis
CO41.3	Solve problems on linear transformations
CO41.4	Use computational techniques and algebraic skills essential for the study of
CO41.4	Eigenvalues and Eigenvectors, and diagonalization

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Textbooks:

- 1. T Veerarajan, Probability, Statistics and Random Processes for Engineers, Tata McGraw Hill, 3rd Edition, 2008
- 2. Gilbert Strang, Linear Algebra and its Applications, Cengage Learning, 4th Edition, 2006 **Reference Books:**
- 1. Richard H Williams, Probability, Statistics and Random Processes for Engineers, Cengage Learning, 1st Edition, 2003
- 2. David C Lay, Linear Algebra and its applications, Pearson, 4th Edition, 2012.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question from each module.**

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. **Some possible AATs:** seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 2.

Table 2: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping															
CO/PO	PO1	P02	P03	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PSO1	PS02	PSO3	PS04
CO41.1	3	2	1									3				
CO41.2	3	2	1									3				
CO41.3	3	2	1									3				
CO41.4	3	2	1									3				
Average	3	2	1									3				

Low-1: Medium-2: High-3

SEMESTER – IV

Course: Principles of Communication Systems(Integrated)

Course Code	22ECE42	CIE Marks	50
Hours/Week (L: T: P)	3:0:2	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Generation and detection of Amplitude modulation.
CLO2	Angle modulation and Demodulation.
CLO3	Noise in Communication systems.
CLO4	Sampling and Quantization techniques.
CLO5	Base band Modulation techniques.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Amplitude Modulation : Introduction, AM- Time domain and frequency domain description, Single Tone Modulation, Generation of AM wave-Switching modulator, Detection of AM waves- Envelop detector. Double Side Band Suppressed Carrier Modulation-Time domain and Frequency	L3
domain description, Generation of DSBSC waves - Ring modulator, Coherent detection of DSBSC modulated wave and Costas loop receiver. (Text-1: 3.1, 3.2 and 3.3)	
Module-2	8 Hours
Sideband Modulation: Single sideband Modulation, Vestigial Side Band Modulation, and frequency Translation. (Text-1: 3.5 and 3.7) Angle Modulation: Introduction, Basic Definitions, Properties of angle Modulated waves, Frequency Modulation- Narrow-Band FM, Wide-Band FM, Transmission bandwidth of FM signal and Generation of FM signals. (Text-1: 4.1, 4.2 and 4.3)	L3
Module-3	8 Hours
Angle Demodulation: Demodulations of FM signals: Balanced frequency discriminator, Phase-Locked Loop, Linear Model of the Phase-Locked Loop and Super Heterodyne Receiver. (Text 1: 4.3, 4.4 and 4.6) Noise in Analog Modulation: Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth, Noise figure, Noise temperature, SNR, Receiver Model, Noise in DSBSC Receivers, Noise in AM receivers and threshold effect. (Text-1: 5.10, 6.2, 6.3, and 6.4)	L3
Module-4	8 Hours
The Transition from Analog to Digital: Introduction, Why Digitize Analog Sources? The Sampling process, Pulse Amplitude Modulation, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves, Bandwidth noise tradeoff, Quantization Process, Quantization Noise. (Text-1: 7.1, 7.2, 7.3, 7.4, 7.6 and 7.8)	L3

Module-5	
Base Band Modulation Techniques: Pulse Code Modulation-Sampling,	
Quantization, Companding-A Law and μ Law Companding, Encoding - line	8 Hours
codes, T1 system, Regeneration, Decoding, Filtering, Multiplexing-: Time	L3
Division Multiplexing and Frequency Division Multiplexing, Delta	
modulation and Delta Sigma Modulation. (Text-1: 7.9, 7.5, 3.8 7 & 7.10)	

Practical Component of IPC					
SI. No.	Experiments	RBT levels			
	List of Experiments to be conducted using Hardware components/ simulation Tools				
1.	Conduct an Experiment to Generate standard Amplitude Modulated wave and demodulate the same	L3, L4			
2.	Conduct an Experiment to generate DSBSC wave and demodulate the same				
3.	Conduct an Experiment to Generate Frequency Modulated wave using 8038 and demodulate the same	L3, L4			
4.	Conduct an Experiment to Generate Pulse Amplitude Modulated wave and demodulate the same	L3, L4			
5.	Conduct an Experiment to Generate Pulse width modulation	L3, L4			
6.	Conduct an Experiment to Generate Pulse position modulation	L3, L4			
7.	Conduct an experiment to Verify sampling theorem	L3, L4			
8.	Simulation of Amplitude modulation and frequency domain analysis using MATLAB	L3, L4			
9.	Simulation of Frequency modulation and frequency domain analysis using MATLAB	L3, L4			
10.	Simulate to verify Sampling theorem using MATLAB	L3, L4			

Course Outcomes: Upon completion of this course, student will be able to:

CO1	Illustrate the process of generation and detection of amplitude modulation techniques used in analog communication systems.
CO2	Apply the concept of angle modulation for generation and detection of FM signals.
CO3	Describe the various types of noises and its performance on modulation techniques.
CO4	Analyze the digital representation of analog signals on modulation techniques.
CO5	Elaborate the operation of base band modulation techniques.

Textbooks:

1. Simon Haykins and Moher, Communication Systems, 5th Edition, John Willey, India Pvt. Ltd, 2010.

Reference books:

- 1. Simon Haykins, An Introduction to Analog and Digital Communication, John Wiley India Pvt. Ltd., 2008
- 2. K. Sam Shanmugam, Digital and Analog Communication systems, Willey, India Pvt. Ltd, 2015.



E-Books / Web References NPTEL Courses

1. https://nptel.ac.in/courses/108/104/108104091/

2. https://nptel.ac.in/courses/108/104/108104098/

Scheme of Evaluation: (Integrated courses)
Scheme of Evaluation: (Integrated courses)

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of four sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question from each module.**

The laboratory assessment of Integrated courses would be restricted to only the CIE evaluation.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. The average of the three tests are taken for computation of CIE on a scale of 30, the CIE would also include laboratory evaluation for 20 marks. The laboratory marks of 20 would comprise of 10 marks for regular laboratory assessment to include lab record and observation. 10 marks would be exclusive for laboratory internal assessment test to be conducted at the end of the semester. The Evaluation pattern for integrated courses is shown in the Table-1

Table-1: Distribution of weightage for CIE & SEE of Integrated courses

	Component	Marks	Total Marks
	CIE Test-1	30	
CIE	CIE Test-2	30	F0
CIE	CIE Test-3	30	50
	Laboratory	20	
SEE	Semester End Examination	100	50
		Grand Total	100

	CO-PO and PSO Mapping													
СО	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	-	-	-	-	-	-	1	-	1	2	1
CO2	3	2	1	-	-	-	-	-	-	1	-	1	2	1
CO3	3	2	1	-	-	-	-	-	-	1	-	1	2	1
CO4	3	2	1	ı	-	-	-	-	-	1	-	1	2	1
CO5	3	2	1	1	-	-	-	1	-	1	_	1	2	1
Average	3	2	1	-	-	-	-	-	-	1	-	1	2	1

Low-1: Medium-2: High-3

SEMESTER – IV

Course: Control Systems

Course Code	22ECE43	CIE Marks	50
Hours/Week (L: T: P)	2:2:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Transforms, Complex Variables, and Special Functions

Course Learning Objectives: Students will be taught;

CLO1	Fundamental concepts and applications of control systems.
CLO2	Mathematical modeling of Mechanical, Electrical, and Electro–Mechanical systems.
CLO3	Time and frequency response of the system.
CLO4	Stability of the system using graphical techniques.
CLO5	Concept of state variable and state model for continuous time systems.

Content	No. of Hours/ RBT levels
Module-1	8 Hours
Introduction to Control Systems: Introduction, Types of Control Systems,	L3
Effect of Feedback Systems, Differential equation of Physical Systems—	
Mechanical Systems, Electrical Systems, Electromechanical systems and	
Analogous Systems. (Text-1: 1.1, 2.1.2.2)	
Module-2	8 Hours
Block diagrams and signal flow graphs: Transfer functions, Block diagram,	L3
algebra, and Signal Flow graphs, Illustrative examples. (Text-1: 2.4 to 2.7)	
Module-3	8 Hours
Time Response of Feedback Control Systems: Introduction, Standard test	L3
signals, Unit step response of First and Second Order Systems. Time	
response specifications, Time response specifications of second order	
systems, Steady state errors, and Error constants. (Text-1: 5.1 to 5.5, 5.7)	
Module-4	8 Hours
Stability analysis: The Concepts of stability, Necessary conditions for	L3
Stability, Routh stability criterion, Relative stability analysis, More on the	
Routh stability criterion.	
Root Locus and Bode plots : Introduction to Root-Locus Techniques, Root	
Locus Concepts, Construction of Root loci and Bode Plots. (Inverse Bode	
Plot Excluded) (Text-1: 6.1 to 6.6, 7.1 to 7.3, 8.4)	
Module-5	8 Hours
Stability in Frequency Domain: Introduction to Polar Plots, (Inverse Polar	L3
Plots excluded) Mathematical preliminaries, Nyquist Stability criterion,	
(Systems with transportation lag excluded).	
Introduction to State variable analysis: Introduction, Concepts of state,	
state variable and state models for electrical systems, Solution of state	
equations. (Text-1: 8.3, 9.1, 9.2, 9.3, 12.1 to 12.3)	

Course Outcomes: Upon completion of this course, student will be able to:

CO1	Explain the concepts of control systems and their applications.
COI	Explain the concepts of control systems and their applications.
CO2	Analyze the mechanical and electrical systems using block diagram reduction
	techniques and Signal Flow graphs to find the overall transfer function.
CO3	Describe quantitative analysis of the transient response of first and second-order
	systems.
CO4	Compute the RH criteria, Root locus, Bode plots, and Nyquist criterion to check the
	stability of the systems.
CO5	Analyze the state variable and state model for continuous time systems.

Textbooks:

1. I.J. Nagrath and M.Gopal, Control Systems Engineering, 5th edition, New Age International(P) Limited, 2011.

Reference Books:

- 1. Benjamin C. Kuo, Automatic Control Systems, 8th edition, John Wiley India Pvt. Ltd., 2008.
- 2. Ogata, Modern Control Engineering, 4th edition, Pearson Education, 2002.

MOOCs:

https://nptel.ac.in/courses/107/106/107106081/ https://nptel.ac.in/courses/108/106/108106098/

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks			
	CIE Test-1	40				
CIE	CIE Test-2	40	F0			
CIE	CIE Test-3	40	50			
	Assignments	10				
SEE	Semester End Examination	50	50			
	Grand Total					



	CO-PO and PSO Mapping													
CO/PO	PO1	P02	PO3	PO4	PO5	P06	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PS02
CO1	1	1	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	2	2	-	-	-	-	-	-	-	-	-	3	2
CO3	2	1	2	-	-	-	-	1	-	-	-	-	2	1
CO4	3	2	2	1	1	-	-	-	-	-	-	1	3	2
CO5	2	2	2	1	1	-	-	-	-	-	-	1	2	2
Average	2	2	2	1	1	-	-	-	-	-	-	1	2	2

Low-1: Medium-2: High-3



SEMESTER – IV

Course: Signals and Systems

Course Code	22ECE44	CIE Marks	50
Hours/Week (L: T: P)	2:2:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Transforms, Complex Variables and Special Functions

Course Learning Objectives: Student will be taught;

CLO1	Mathematical description of continuous and discrete time signals and systems
CLO2	LTI Systems and properties
CLO3	Fourier Representation of Signals and LTI Systems
CLO4	Non periodic signals using Fourier Transforms.
CLO5	Z-Transforms and its properties.

Content	No. of Hours/ RBT levels
Module-1	8 Hours
Introduction and Classification of signals: Definition of signal and	L2
systems, Classification of signals.	
Basic Operations on signals: Amplitude scaling, addition, multiplication,	
differentiation, integration, time scaling, time shift and time reversal.	
Elementary signals/Functions : Exponential, sinusoidal, step, impulse, and	
ramp functions.	
Module-2	8 Hours
Properties of Systems: Linear-nonlinear, Time variant-invariant, causal, non-causal, static-dynamic, stable-unstable, invertible.	L3
Time domain representation of LTI Systems: Impulse response,	
convolution sum, convolution integral. Computation of convolution sum	
and convolution integral using graphical method for unit step and unit	
step, unit step and exponential.	
Module-3	8 Hours
Fourier Representation of Signals and LTI Systems: Discrete- Time	L3
Periodic Signals: The Discrete-Time Fourier Series, Continuous-Time	
Periodic Signals: The Fourier Series, basic problems. CTFS and DTFS	
properties (Analytical treatment).	
Module-4	8 Hours
Fourier Representation of Non-Periodic Signals: Introduction, Discrete-	L3
Time Non-Periodic Signals: The Discrete-Time Fourier Transform,	
Continuous-Time Non-Periodic Signals: The Fourier Transform, Inverse	
Fourier Transforms.	
Properties of Fourier Transform (Analytical treatment), problems on	
properties of Fourier Transform.	
Module-5	8 Hours
Z-Transforms : Z-transform, properties of the Region of Convergence,	L3
properties of the Z-transform, Inverse Z-transforms, unilateral Z-	
transform and Transform Analysis of LTI systems-pole-Zero plots, causality	
and stability in terms of Z- transforms	

Course Outcomes: Upon completion of this course, student will be able to:

CO1	Solve the both Continuous time Discrete time signals with various operations.
CO2	Compute the response of a Continuous and Discrete LTI system using convolution
	integral and convolution sum.
CO3	Analyze the frequency response of a given arbitrary periodic CTS/ DTS using
	Fourier series and its properties.
CO4	Determine frequency response of a given arbitrary Non-periodic CTS/DTS using
	Fourier transforms and its properties.
CO5	Compute the Z-transforms, inverse Z- transforms and transfer functions of
	complex LTI systems.

Textbooks:

1. Simon Haykin and Barry Van Veen, Signals and Systems, 2nd edition, Wiley India. 2008.

Reference books:

- 1. Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab, Signals and Systems, 2nd edition, Pearson Education, 2002.
- 2. Michael Roberts, Fundamentals of Signals and Systems, 2nd edition, Tata McGraw-Hill, 2010

NPTEL:

- 1. https://nptel.ac.in/courses/108/104/108104100/
- 2. https://nptel.ac.in/courses/108/106/108106163/
- 3. https://nptel.ac.in/courses/117/101/117101055/

MOOCs

https://ocw.mit.edu/resources/res-6-007-signals-and-systems-spring-2011/

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks			
	CIE Test-1	40				
CIE	CIE Test-2	40	F0			
CIE	CIE Test-3	40	50			
	Assignments	10				
SEE	Semester End Examination	50	50			
	Grand Total					



	CO-PO & PSO Mapping													
CO/PO	PO1	P02	P03	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PS01	PS02
CO1	1	1	-	-	-	-	-	-	1	-	-	1	-	-
CO2	3	1	-	1	-	-	-	-	1	-	ı	1	2	1
CO3	2	1	-	-	-	-	-	-	-	-	-	1	2	1
CO4	3	1	-	-	-	-	-	-	-	-	-	1	2	1
CO5	3	1	-	-	-	-	-	-	-	-	-	1	2	1
Average	3	1	-	-	-	-	-	-	1	-	-	1	2	1

Low-1: Medium-2: High-3



SEMESTER – IV

Course: Data Structures Using C++

Course Code	22ECE45	CIE Marks	50
Hours/Week (L: T: P)	2:0:2	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Objectives: Students will be taught.

CLO1	Types of data structures, Searching and sorting Algorithms.
CLO2	concepts of dynamic memory allocation and linked lists.
CLO3	Stack and Queues, its primitive operations.
CLO4	Binary trees representation.
CLO5	Graph representation and implementation of Shortest path algorithms.

Content	No. of Hours/ RBT levels
Module 1	
Introduction: Data Structures, Classifications (Primitive & Non-Primitive), Data structure Operations.	
Searching: linear search, binary search, recursive binary search.	
Sorting: Bubble sort, selection sort, insertion sort, quick sort, binary tree sort,	8 Hours
merge sort, heap sort. ((Text 1: 6.1, 6.2, Text 2: Chapter 9 full)	L2
Module 2	8 Hours
Dynamic Memory Allocation: Introduction, Dynamic Memory Allocation, Allocating a Block of Memory: malloc, Allocating multiple blocks of Memory: calloc, Releasing the Used Space: Free, Altering size of the block: realloc, Linked List: What is linked list, operation on linked list, more linked lists, reversing the links, A few more operations, Recursive operations on linked lists, Doubly linked lists. (Text 1: Chapter 6.3, Text 2: Chapter 3 full)	L3
Module 3	
Stacks: stack as an array, stack as a linked list, Applications of stacks, Infix to postfix conversion, postfix to prefix conversion, other interconversions, Evaluation of postfix expression.	8 Hours L3
Queues: Queue as an array, Queue as a linked list, circular Queue, Deque, priority queue. (Text 2: Chapter 5 and 6 full).	
Module 4	8 Hours
Trees: Binary Trees, Representation of binary trees in memory, Linked	L3
representation of binary trees, Array representation of binary trees, Binary	
search trees, Operations on binary search trees, Reconstruction of binary tree,	
Threaded Binary trees, AVL Trees, Binary Heap. (Text 2: Chapter 7 full)	
Module 5	8 Hours
Graphs: Definition and terminology, graph representations, graph traversal, spanning tree, shortest path, topological sorting. (Text 2: Chapter 8 full)	L2

COURSE OUTCOMES: Upon completion of this course, student will be able to;

CO1	Comprehend different types of data structures and apply algorithms to perform
	searching and sorting
CO2	Discribe primitive operations on linked lists.
CO3	Explain the operational aspects of stacks and queues.
CO4	Implement operations on Binary Trees.
CO5	Implement shortest path algorithms using graphs.

Text Books:

- 1. Seymour Lipschutz, Data Structures with C, Schaum's Outlines, Special Indian Edition, 13th reprint, Tata McGraw Hill Education, 2015.
- 2. Data Structures Through C++, Yashavant P Kanetkar, 3rd Edition, BPB Publication.

References:

- 1. D. S. Malik, Data Structures Using C++, 2nd edition, Cengage Learning.
- 2. Varsha H Patil, Data Structures Using C++, Oxford University Press, 2012

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE and SEE of Regular courses

	0 0		
	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	Grand Total		100

	CO-PO and PSO Mapping													
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	-	-	-	-	1	-	-	-	1	-	2
CO2	3	3	3	-	-	-	-	1	-	-	-	1	-	2
CO3	3	3	3	-	-	-	-	1	-	-	-	1	-	2
CO4	3	3	3	-	-	-	-	1	-	-	-	1	-	2
CO5	3	3	3	-	-	-	-	1	1	-	_	1	-	2
Average	3	3	3	-	-	-	-	1	1	-	-	1	-	2

Low-1: Medium-2: High-3

SEMESTER – IV

Course: Verilog HDL

Course Code	22ECE46	CIE Marks	50
Hours/Week (L: T: P)	3:0:2	SEE Marks	50
No. of Credits	4	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Different modeling concepts in Verilog.
CLO2	Verilog based design using Gate Level and Data Flow Modeling Styles.
CLO3	Behavioral description, Tasks and Functions in Verilog.
CLO4	Programming concept for Digital Circuits using state machine charts.
CLO5	Logic Synthesis and its effects in Verification.

Content	No. of Hours /
	RBT levels
Module-1	8 Hours
Overview of Digital Design with Verilog HDL: Evolution of CAD,	L1, L2
emergence of HDLs, typical HDL-flow, why Verilog HDL? trends in HDLs.	
Hierarchical Modeling Concepts: Top-down and bottom-up design	
methodology, differences between modules and module instances, parts	
of a simulation, design block, stimulus block. (Text 1: 1.1 to 1.6, 2.1 to 2.6)	
Basic Concepts: Lexical conventions, data types, system tasks, compiler	
directives. Modules and Ports: Module definition, port declaration,	
connecting ports. (Text 1: 3.1 to 3.3, 4.1 to 4.2)	
Module-2	8 Hours
Gate-Level Modeling: Gate Types, Gate Delays: rise, fall and turn-off	L1, L2
delays, min, max, and typical delays, Delay Example (Text 1: 5.1 and 5.2)	
Dataflow Modeling: Continuous assignments, delay specification,	
expressions, operators, operands, operator types, Examples :4 to 1 MUX,	
4 Bit Full adders: Full adder data flow model, full adder with carry look	
ahead-Verilog Programs. (Text 1: 6.1 to 6.5)	
Module-3	8 Hours
Behavioral Modeling: Structured procedures, initial and always, blocking	L1, L2
and non-blocking statements, conditional statements, Multiway	
branching, loops. (Text 1: 7.1 to 7.2 and 7.4 to 7.6)	
Tasks and Functions : Differences between tasks and functions, Task:	
Declaration and Invocation-Syntax, Task Example. Function: Declaration-Syntax, Example-Parity calculation(Text 1: 8.1 to 8.3)	
Module-4	8 Hours
Design Examples: BCD to 7 segment Display Decoder, Traffic Light	L2, L3
Controller, Synchronization and Debouncing, Shift and Add Multiplier:	
Design and Verilog program, Signed/Fraction Multiplier-Design and	
Verilog program. (Text 2 :4.1, 4.4, 4.7, 4.8 &4.10)	
State Machine Charts: SM Charts, Derivation of SM Charts: Binary	
Multiplier, Dice Game-SM chart Realization of SM Charts. (Text 2:5.1 and	
5.2)	



Module-5	8 Hours
Modeling Techniques: Procedural Continuous Assignments, Overriding	L2, L3
Parameters, Conditional Compilation and Execution, Time Scales. (Text 1:	
9.1 to 9.4)	
Logic Synthesis with Verilog: Logic Synthesis, Impact of Logic Synthesis,	
Verilog HDL Synthesis, Synthesis Design Flow and Verification of Gate	
Level Netlist. (Text 1:14.1 to 14.5)	

Course Outcomes: Upon completion of this course, student will be able to:

CO1	Analyze the Verilog programs using different abstract levels.
CO2	Design and Verify the functionality using test benches.
CO3	Develop a Verilog program with tasks and functions.
CO4	Apply the SM Charts to realize the digital circuits.
CO5	Interpret the verification of digital circuit using logic synthesis.

Textbooks:

- 1. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Pearson Education, 2nd Edition, Reprint 2020.
- 2. Charls H. Roth Jr, Lizy K, John and Byeong K. Lee, Digital Systems Design Using Verilog, Cengage Learning,1st Edition, 2016.

Reference Books:

- 1. Michel D. Ciletti , Advanced Digital Design with the Verilog HDL, Pearson Education, 2nd Edition, 2011.
- 2. Peter J. Ashenden, Digital Design: An Embedded Systems Approach using Verilog, Elsevier, 2015.
- 3. Stephen Brown and Zvonkoc Vranesic, Fundamentals of Digital Logic with Verilog Design, Mc-Graw Hill Publication, 2003,

MOOCs

https://www.mitzon.com/mooc/digital-design-using-verilog-hdl-programming-with-practical/

https://www.coursera.org/learn/fpga-hardware-description-languages

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1



Table 1: Distribution of weightage for CIE and SEE of Regular courses

	Component	Marks	Total		
			Marks		
	CIE Test-1	40			
CIE	CIE Test-2	40	F0		
	CIE Test-3	40	50		
	Assignments	10			
SEE	Semester End Examination	50	50		
	100				

CO-PO and PSO mapping														
CO/PO	P01	P02	PO3	P04	P05	P06	P07	P08	P09	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	2	3		1			1	2	1	2	1	2	2
CO2	3	2	3					1	2	1	2	1	2	2
CO3	3	2	3	2	3			1	2	1	2	1	2	2
CO4	3	2	3	1	3			1	2	1	2	1	2	2
CO5	2	2	2	3	3			1	2	1	2	1	2	2
Average	3	2	3	3	3			1	2	1	2	1	2	2

Low-1: Medium-2: High-3



SEMESTER - IV

Course: HDL Laboratory

Subject Code	22ECEL47	CIE Marks	50
Hours/Week (L: T: P)	0:0:2	SEE Marks	50
Credits	1	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Dataflow modeling style in Verilog
CLO2	Implementation of Behavioral and structural modeling style in Verilog HDL.
CLO3	Verification of combinational and sequential circuits using simulator
CLO4	Simulation of Test bench using simulator.

	List of Experiments								
Wr	Write a Verilog Code to verify the functionality of the following Digital Circuits using								
sim	simulation CAD tool(Xilinx) or cadence tool.								
1	Full Adder Circuit using Two Half adders.								
2	2 to 4 Decoder using NAND Gates only (Structural model)								
3	8 to 3 Encoder with priority & without priority (Behavioral Model)								
4	8 to 1 Multiplexer using case statements and if statements.								
5	4-bit Binary to Gary Code converter.								
6	SR, D and JK flip-flops.								
7	4-bit Binary Counter.								
8	4- bit BCD counter.								
9	8- bit ALU to perform addition, subtraction, multiplication and logical operations.								
10	4- bit Ripple carry adder using structural model.								

Course Outcomes: Upon successful completion of this course, student will be able to:

CO1	Develop Verilog HDL code for combinational circuits.
CO2	Verify sequential circuits using modelsim simulator.
CO3	Analyze the digital circuits using test bench.
CO4	Apply sequential statements to implement digital circuits.
CO5	Apply Structural modeling style to digital circuits.

Textbook:

1. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Pearson Education, 2nd Edition, Reprint 2020.

Scheme of Examination:

Semester End Examination (SEE):

All laboratory experiments are to be included for practical examination. Students can pick one experiment from the questions lot prepared by the examiners. Change of experiment is allowed only once and 15% Marks allotted to the write up part to be made zero.

Semester End Examination Evaluation							
SL.NO	ACTIVITY	MARKS					
1	Write-Up	15					
2	Conduction	70					
3	Viva Voce	15					
	TOTAL	100					

Note: The marks scored will be proportionately reduced to 50

25

Continuous Internal Evaluation (CIE):

As part of CIE process, progressive continuous evaluation is done for laboratory work on weekly basis of conduct of experiment by student either individually or in group based on the laboratory. The breakup of the marks allocated is given in the TABLE-1

	7 1					
TABLE-1 WEEKLY EVALUATION OF CONDUCT OF EXPERIMENT						
SL.NO	ACTIVITY	MAX MARKS				
1	Conduct of experiment and documentation	10				
2	Analysis & interpretation of results	5				
3	Viva voce	5				
	TOTAL					

Internal examination is conducted at the end of the semester or on completion of a predefined set of experiments based on the laboratory. The evaluation detail of laboratory internal exam is given in TABLE-2

TABLE-2 LAB INTERNAL EXAMINATION							
SL.NO	ACTIVITY	MAX MARKS					
1	Detailed write-up about the experiment with relevant procedure and calculation.	5					
2	Conduction of experiment	20					
3	Viva voce	5					
	TOTAL						

	TABLE-3 FINAL CIE CALCULATION							
SL.NO	SL.NO METRICS USED							
1	Average of all weekly evaluation of conduct of experiment	20						
2	Class Internal Examination	30						
	TOTAL							

	CO-PO and PSO Mapping													
CO/PO	P01	P02	P03	P04	P05	P06	P07	P08	P09	PO10	P011	P012	PS01	PS02
CO1	3	3	2	-	1	-	-	-	1	-	-	1	2	1
CO2	3	3	2	-	1	-	-	-	1	-	-	1	2	1
CO3	3	3	2	-	1	-	-	1	1	1	-	1	2	1
CO4	3	3	2	-	1	-	-	ı	1	ı	-	1	2	1
CO5	3	3	2	-	1	-	-	1	1	1	-	1	2	1
Average	3	3	2	-	1	_	-	ı	1	ı	-	1	2	1

Low-1: Medium-2: High-3





III- YEAR ECE SYLLABUS-2022 SCHEME



Department of Electronics and Communication Engineering

GLOBAL ACADEMY OF TECHNOLOGY

(Autonomous institution affiliated to VTU, Belagavi.

Accredited by NAAC with 'A' grade,

NBA Accredited CS, E&C, E&E, MECH, CV and IS branches)

Ideal Homes Township,

Raja Rajeshwari Nagar, Bengaluru-560098.

Global Academy of Technology, Bengaluru

(Autonomous Institution Affiliated to VTU)

Scheme of Teaching and Examination 2022-23

Electronics and Communication Engineering

V SEMESTER -UG

SI.	Course Code	ourse Code Course Title		Course Teaching Dept.		eachir urs/W		Examination			CREDITS
No.			Туре		L	Т	Р	CIE	SEE	Total	
1	22ECE51	Engineering Economics and Management	PC		3	0	0	50	50	100	3
2	22ECE52	Digital Communication Systems (Integrated)	IPC	Respective	3	0	2	50	50	100	4
3	22ECE53	Digital Signal Processing	PC	Department	3	2	0	50	50	100	3
4	22ECE54	Engineering Electromagnetics	PC		2	2	0	50	50	100	3
5	22ECE55X	Program Elective-1	PEC	PEC		0	0	50	50	100	3
6	22ECE56	Programming in Java	AEC		2	0	0	50	50	100	2
	22CIV57	Environmental Science	CV	Civil							
7		OR			1	0	0	50	50	100	1
	22UHV57	Universal Human Values	BS	Respective Department							
8	22ECEL58 Digital Signal PCL Processing Laboratory			0	0	2	50	50	100	1	
	TOTAL 350 350 800 20										

Program Elective-1*								
22ECE551	Operating Systems	22ECE553	Power Electronics					
22ECE552	Nanoelectronics	22ECE554	Satellite Communication					

*NPTEL for Credit transfer: Students can take 12 weeks NPTEL course as an equivalent to Program elective. The NPTEL courses of duration less than 12 weeks will not be considered for credit transfer. The courses (only technical) taken are as per the recommendation of BOS of respective department. The similarity of the contents as offered by NPTEL should not exceed a maximum of 40% of the courses being registered by the student. The NPTEL course need to be completed before the registration of the elective. Any certificate obtained after the registration of elective would not be considered. The validity of NPTEL certificate is for two years and it cannot be used more than once to avail the benefit. The student is eligible to transfer a maximum of nine credits in the entire duration of the program. The grades will be awarded as equivalent to the grades obtained in the NPTEL course.



Global Academy of Technology, Bengaluru

(Autonomous Institution Affiliated to VTU)

Scheme of Teaching and Examination 2022-23 Electronics and Communication Engineering

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SI.	Course Code	Course Title	Course	Teaching	Teaching Hours/Week			Examination			CREDITS
No.			Туре	Dept.	L	Т	Р	CIE	SEE	Total	
1	22ECE61	Information Theory and Coding	PC		3	0	0	50	50	100	3
2	22ECE62	ARM Controller (Integrated)	IPC	Respective Department	3	0	2	50	50	100	4
3	22ECE63	VLSI Design	PC	,	3	0	0	50	50	100	3
4	22ECE64X	Program Elective-2	PEC		3	0	0	50	50	100	3
5	22ECE65X	Open Elective-1	OEC	Offering Department	3	0	0	50	50	100	3
	22CIV66	Environmental Science	HSM	Civil							
6		OR				0	0	50	50	100	1
	22UHV66	Universal Human Values	BS	Respective Department							
7	22ECEL67	VLSI Laboratory	PCL	Respective Department	0	0	2	50	50	100	1
8	22ECEMP68	Mini Project	MP	Respective Department	hc	Two Contact hours per week		50	50	100	2
	TOTAL 350 350 800 20									20	

Program Elective-2								
22ECE641	Speech Signal Processing	22ECE643	Micro Electro Mechanical Systems					
22ECE642	Digital Image Processing	22ECE644	Microwave and Radar					
	Open Elective-1 (Offered	to other bra	nch students)					
22ECE651	Communication Engineering	22ECE653	Microcontroller and its Applications					
22ECE652	Electronic Circuits with Verilog	22ECE654	Internet of Things					

*NPTEL for Credit transfer: Students can take 12 weeks NPTEL course as an equivalent to Program elective. The NPTEL courses of duration less than 12 weeks will not be considered for credit transfer. The courses (only technical) taken are as per the recommendation of BOS of respective department. The similarity of the contents as offered by NPTEL should not exceed a maximum of 40% of the courses being registered by the student. The NPTEL course need to be completed before the registration of the elective. Any certificate obtained after the registration of elective would not be considered. The validity of NPTEL certificate is for two years and it cannot be used more than once to avail the benefit. The student is eligible to transfer a maximum of nine credits in the entire duration of the program. The grades will be awarded as equivalent to the grades obtained in the NPTEL course.



SEMESTER - V

Course: Engineering Economics and Management

Course Code	22ECE51	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Importance of management and planning
CLO2	Characteristics of organization and leadership Styles.
CLO3	Importance of project management
CLO4	Fundamentals of economic concepts and value of money.
CLO5	Breakeven analysis and risk analysis.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Management: Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession. Planning: Nature, Importance and Purpose of Planning, Types of Plans, Steps in Planning, Limitations of Planning, Decision Making – Meaning, Types of Decisions-Steps in Decision Making. (Text 1)	L2
Module-2	8 Hours
Organizing and Staffing: Meaning, Characteristics of Organization — Process of Organization, Principles of Organization, Span of Management, Departmentalization, Meaning, Process of Departmentalization, Purpose of Departmentalization, Committees — meaning, Types of Committees, Importance of Staffing, Manpower planning, Sources of Recruitment, Process of Selection. Directing and Controlling: Meaning, Requirement of Effective Direction, Giving order, Motivation. Communication — Meaning and Purpose of communication Coordination- Meaning and Need, Types and Techniques of Coordination. Controlling — Meaning, Steps in Controlling. (Text 1)	L2
Module-3	8 Hours
Leadership: Meaning, Characteristics of Leadership, Functions of Executive Leader, Traditional Approaches to Leadership. Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance. (Text 1)	L3
Module-4	8 Hours
Introduction to Engineering Economy: Introduction, Problem solving and decision making, Engineering Economic Decision Maze. Time Value of Money: Interest and value of money, Reasons for interest, Simple interest, Compound interest, Compound interest factors, Cash flow diagram, Calculation of time-value Equivalences. (Text 2)	L3



Module-5	
Break Even Analysis: Basic concepts, Linear break-even analysis, break even	8 Hours
charts, algebraic relationships, break-even point alternatives, dumping,	L2
multiproduct alternatives and multiple alternatives, Nonlinear Break-even	
analysis: marginal revenue and profit, marginal cost and average unit cost,	
Inflation and its effects, Inflation, its causes and consequences. Effects of inflation	
on Breakeven Analysis.	
Risk Analysis: Recognizing Risk, Including risk in Economic Analyses, Probability	
concepts for economic Analysis, Applications of Probability concepts. (Text 2)	

CO 1	Explain the importance of Management and Planning
CO 2	Describe the characteristics of organization and direction
CO 3	Discuss the fundamentals of leadership styles and Social Responsibility of Business
CO 4	Understand the concept of Engineering Economics and Time value of Money.
CO 5	Explain the concepts Break-Even Analysis and Risk analysis

Textbooks:

- 1. Principles of Management P.C. Tripathi, P.N.Reddy McGraw Hill, 6th Edition, 2017
- 2. Engineering Economics by, James L. Riggs, David D. Bedworth, Sabah U. Randhawa McGraw Hill Education, 4th Edition, 2004.

Reference Books:

1. Essentials of Management: An International, Innovation and Leadership perspective Harold Koontz, Heinz Weihrich McGraw Hill 10thEdition 2016

E-Books / Web References:

https://www.youtube.com/watch?v=8GFXOWxlySs

MOOCs:

https://onlinecourses.nptel.ac.in/noc20 mg58/preview

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1



Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component Marks					
	CIE Test-1	40				
CIE	CIE Test-2	40	F0			
CIE	CIE Test-3	40	- 50			
	Assignments	10				
SEE	Semester End Examination	50	50			
	Grand Total					

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	-	-	-	1	-	-	-	1	-	-
CO2	2	-	-	-	-	-	-	1	-	-	ı	1	-	-
CO3	2	-	-	-	-	-	-	1	-	-	-	1	-	-
CO4	2	-	-	-	-	-	-	1	-	-	ı	1	-	-
CO5	2	ı	ı	ı	-	ı	ı	1	ı	ı	ı	1	-	-
Average	2	-	-	-	_	-	-	1	-	-	1	1	-	-

Low-1: Medium-2: High-3



SEMESTER - V

Course: Digital Communication Systems (Integrated)

Course Code	22ECE52	CIE Marks	50
Hours/Week (L: T: P)	3:0:2	SEE Marks	50
No. of Credits	4	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Representation of baseband signals and line codes.
CLO2	Signals over AWGN Channels, optimum receivers.
CLO3	Digital Modulation Techniques.
CLO4	Data Transmission through band limited channels.
CLO5	Principles of Spread Spectrum.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Bandpass Signal to Equivalent Low pass: Hilbert Transform, Pre-envelopes,	L3
Complex envelopes, Canonical representation of bandpass signals, Complex low	
pass representation of bandpass systems, Complex representation of band pass	
signals and systems. (Text 1: 2.8, 2.9, 2.10, 2.11, 2.12)	
Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power	
spectral densities. (Text 1: 6.10)	
Overview of HDB3, B3ZS, B6ZS (Reference Text 1: 7.2.5)	
Module-2	8 Hours
Signalling over AWGN Channels: Introduction, Geometric representation of signals,	L3
Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN	
channel into a vector channel, Optimum receivers using coherent detection: ML	
Decoding, Correlation receiver, matched filter receiver (Text 1: 7.1 to 7.4).	
Module-3	8 Hours
Digital Modulation Techniques: Phase shift Keying techniques using coherent	L3
detection: generation, detection, and error probabilities of BPSK and QPSK, M-ary	
PSK, M-ary QAM, Frequency shift keying techniques using Coherent detection: BFSK	
generation, detection and error probability.	
Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol	
representation, Block diagrams treatment of Transmitter and Receiver, Probability	
of error (without derivation of probability of error equation) (Text 1: 7.6, 7.7 & 7.8)	
Module-4	8 Hours
Communication through Band Limited Channels: Digital Transmission through	L3
Band limited channels: Digital PAM Transmission through Band limited Channels,	
Signal design for Band limited Channels: Design of band limited signals for zero ISI-	
The Nyquist Criterion (statement only), Design of band limited signals with	
controlled ISI-Partial Response signals,	
Probability of error for detection of Digital PAM: Probability of error for detection	
of Digital PAM with Zero ISI, Symbol-by-Symbol detection of data with controlled	
ISI	
Channel Equalization: Linear Equalizers (Text 2: 10.1, 10.2, 10.3, 10.4 & 10.5.2)	
Module-5	8 Hours

Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model	L2, L3
of a Spread Spectrum Digital Communication System, Direct Sequence Spread	
Spectrum Systems, Effect of De-spreading on a narrowband Interference,	
Probability of error (statement only), Some applications of DS Spread Spectrum	
Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA	
based on IS-95 (Text 2: 15.1, 15.2, 15.3, 15.4 & 15.5)	

	Practical Component of IPC						
	List of Experiments						
1	Conduct an experiment to generate FSK and PSK modulated signals and demodulate the same.						
2	Conduct an experiment to Measure of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.						
3	Conduct an experiment to Obtain the Radiation Pattern and Measurement of directivity and gain of micro strip dipole and Yagi antennas.						
4	Conduct an experiment to Determine: a. Coupling and isolation characteristics of micro strip directional coupler. b. Resonance characteristics of micro strip ring resonator and computation of dielectric constant of the substrate. c. Power division and isolation of micro strip power divider.						
5	Simulate NRZ, RZ, half-sinusoid and raised cosine pulses and generate eye diagram for binary polar signaling using MATLAB.						
6	Simulate Pulse code modulation and demodulation system using MATLAB.						
7	Simulate Computations of the Probability of bit error for coherent binary ASK, FSK and PSK for an AWGN Channel and compare them with their Performance curves using MATLAB.						
8	Simulate Digital Modulation Schemes i) DPSK Transmitter and receiver, ii) QPSK Transmitter and Receiver using MATLAB.						

	1 1
CO1	Represent the signals in various forms.
CO2	Explain the concept of source and channel coding techniques.
CO3	Generate and detect various Digital Modulation techniques.
CO4	Compute performance parameters of band limited channels.
CO5	Explain the concept of Spread spectrum communication system.

Textbooks:

- 1. Simon Haykin, Digital Communication Systems, 1st edition, John Wiley & sons, 2014.
- 2. John G Proakis and Masoud Salehi, Fundamentals of Communication Systems, 2nd edition, Pearson Education, 2014.

Reference Books:

- 1. B.P. Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, 4th Edition, Oxford University Press, 2010.
- 2. Ian A Glover and Peter M Grant, Digital Communications, 3rd Edition, Pearson Education, 2010.
- 3. Bernard Sklar and Ray, Digital Communications Fundamentals and Applications, 3rd edition, Pearson Education, 2014.

Scheme of Evaluation: (Integrated courses)

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of four sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question from each module.**

The laboratory assessment would be restricted to only the CIE evaluation.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. The average of the three tests are taken for computation of CIE on a scale of 30, the CIE would also include laboratory evaluation for 20 marks. The laboratory marks of 20 would comprise of 10 marks for regular laboratory assessment to include lab record and observation. 10 marks would be exclusive for laboratory internal assessment test to be conducted at the end of the semester. Typical Evaluation pattern for integrated courses is shown in the Table1

Table1: Distribution of weightage for CIE & SEE of Integrated courses

	3 3		
	Component	Marks	Total Marks
	CIE Test-1	30	
CIE	CIE Test-2	30	F0
CIE	CIE Test-3	30	50
	Laboratory	20	
SEE	Semester End Examination	100	50
		Grand Total	100

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	P04	PO5	P06	PO7	P08	P09	PO10	PO11	PO12	PS01	PS02
CO1	3	2	1	-	-	-	-	ı	-	-	-	3	2	2
CO2	3	2	1	1	1	-	-	ı	1	1	1	3	2	2
CO3	3	2	1	ı	1	-	-	ı	1	1	1	3	2	2
CO4	3	2	1	-	-	-	-	1	-	-	-	3	2	2
CO5	3	2	1	1	1	-	-	ı	-	1	1	3	2	2
Average	3	2	1	1	-	-	-	. 1	-	1	1	3	2	2

Low-1: Medium-2: High-3

SEMESTER - V

Course: Digital Signal Processing

Course Code	22ECE53	CIE	50
Hours/Week(L:T:P)	3:2:0	SEE	50
No. of Credits	4	Examination Hours	03

Prerequisites: Signals and systems

Course Learning Objectives: Students will be taught:

	U ,
CLO1	Frequency domain sampling and reconstruction of discrete-time signals and
	their properties.
CLO2	DFT and its properties.
CLO3	FFT algorithms and linear filtering approach.
CLO4	Digital IIR filters and their realization.
CLO5	Digital FIR filters and their realization.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals. DFT as a linear transformation its relationship with other transforms. Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular convolution. (Text 1: 7.1, 7.2.1, 7.2.2)	L3
Module-2	8 Hours
Additional DFT properties: Time Reversal, Circular Time Shift, Circular Frequency Shift, Complex Conjugate & Parseval's Theorem. Use of DFT in Linear Filtering: Overlap-save and overlap-add method. Direct computation of DFT, Need for Efficient Computation of the DFT (FFT algorithms). (Text 1: 7.2.3, 7.3 & 8.1.1)	L3
Module-3	8 Hours
Fast Fourier Transform (FFT) algorithms: Radix-2 FFT algorithms for the computation of DFT and IDFT — Decimation in Time and Decimation in Frequency algorithms. Goertzel algorithm, and Chirp Z Transform. (Text 1: 8.1.3, 8.3)	L3
Module-4	8 Hours
Analog filters: Characteristics of commonly used analog filters – Butterworth and chebyshev filters, Design of analog filter, frequency transformations in analog domain.: (Text 1: 10.3.4, 10.3.1, 10.3.2, 10.3.3, 10.3.5, 10.4.1) Digital IIR Filter: Analog to Digital transformations; Impulse invariance Technique, Bilinear transformation. Design of digital IIR Filters using Impulse invariance and Bilinear transformation. (Text 1:10.3.2, 10.3.3) Structure for IIR Systems: Direct Form-I, Direct form-II, Cascade form, Parallel form structures. (Text 1: 9.3.1, 9.3.3, 9.3.4)	L4
Module-5	8 Hours
FIR Filters : Characteristics of practical frequency selective filters, Symmetric and anti-symmetric FIR filters, Window functions: Rectangular, Hanning and Hamming, Design of FIR filters using Rectangular, Hamming and Hanning,	L2

Blackmann and Kaiser. Design of Linear Phase FIR filters by Frequency sampling method. (Text 1:10.1.2, 10.2.1, 10.2.2, 10.2.3)

Realization of FIR Filter: Direct Form I & II, Cascade form, and Lattice structures. (Text 1:9.2.1, 9.2.2, 9.2.4.)

Course Outcomes: Upon completion of this course, students will be able to:

CO1	Describe the frequency domain sampling and reconstruction of DT signals and its
	properties.
CO2	Evaluate the DFT using properties.
CO3	Compute DFT using FFT algorithms and linear filtering approach.
CO4	Design and implementation of FIR filters.
CO5	Design and implementation of IIR filters.

Textbook:

1. Johan G. Proakis and Dimitris G. Manolakins, "Digital Signal Processing —Principles, Algorithms and Applications", Fourth Edition, Pearson Education, New Delhi, 2007.

Reference Books:

1. Sanjit K Mithra, Digital signal Processing, A Computer Based approach, 4th edition, McGraw Hill Education, 2013.

MOOCs:

https://nptel.ac.in/courses/117102060 https://nptel.ac.in/courses/108106151

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question from each module.**

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. CIE is executed by way of two quizzes /Alternate Assessment Tools (AATs) and three tests. **Some possible AATs:** seminar/assignments/ mini projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern is shown in Table 1.

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks			
	CIE Test-1	40				
CIE	CIE Test-2	40	50			
CIE	CIE Test-3	40	50			
	Assignments	10				
SEE	Semester End Examination	50	50			
	Grand Total					

	CO-PO & PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	-	1	1
CO2	3	2	2	-	-	-	-	-	-	-	-	1	1	1
CO3	3	2	2	-	-	1	-	-	-	-	-	1	2	2
CO4	3	2	2	ı	1	1	-	1	-	1	-	1	2	2
CO5	3	2	2	-	-	ı	-	-	-	-	_	1	2	2
Average	3	2	2	-	-	ı	-	-	-	-	-	1	2	2

Low -1: Medium -2: High-3



SEMESTER - V

Course: Engineering Electromagnetics

Course Code	22ECE54	CIE Marks	50
Hours/Week (L: T: P)	2:2:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Vector Algebra

Course Learning Objectives: Students will be taught;

CLO1	Coulomb's Law, Electric Field Intensity and Flux density.
CLO2	Gauss's law and Divergence.
CLO3	Electric and magnetic field parameters using various static Electromagnetic
	Laws.
CLO4	Maxwell's equations for static and time varying Fields.
CLO5	Concept of Uniform Plane waves.

Content Module-1 Coulomb's Law, Electric Field Intensity and Flux density: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field of sheet of charge & Electric flux density. (Text-1: 2.1 to 2.5 and 3.1)	No.of Hours/ RBT levels 8 Hours L3
Module-2 Gauss's law and Divergence: Gauss' law, Application of Gauss law: Some Symmetrical Charge Distributions, Applications of Gauss Law: Differential Volume Element, Divergence, Maxwell's First equation, Vector Operator del & Divergence theorem. (Text-1: 3.2 to 3.7) Energy, Potential and Conductors: Energy expended in moving a point charge in an electric field, The line integral, Definition of potential difference and potential & The potential field of point charge. (Text-1: 4.1 to 4.4)	8 Hours L3
Module-3 Steady Magnetic Field: Current and Current density, Continuity of current. Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem, Magnetic flux and magnetic flux density, Scalar and Vector Magnetic Potentials. (Text-1: 5.1, 5.2 and 8.1 to 8.5)	8 Hours L3
Module-4 Magnetic Forces and Maxwell's Equations: Force on a moving charge, differential current elements, Force between differential current elements - Numerical Problems. Faraday's law, displacement current, Maxwell's equations in point form, Maxwell's equations in integral form for static and time varying fields. (Text-1: 9.1, 9.2, 9.3, 10.1 to 10.4)	8 Hours L3

Module-5	
Uniform Plane Wave: Wave propagation in free space, Wave propagation in	8 Hours
Dielectrics, Poynting's Theorem, Propagation in good conductors: Skin effect.(Text-1: 12.1 to 12.4)	L3

CO1	Apply the concept of Coulomb's law and Electric field Intensity to determine
	Electrostatic force and Field
CO2	Apply Guass's law, Divergence and potential to solve problems on various charge
	distributions.
CO3	Analyze different laws of Steady magnetic field to solve engineering Problems.
CO4	Explain magnetic forces and Maxwells equations.
CO5	Discuss wave propagation in various media.

Textbooks:

1. W.H. Hayt and J.A. Buck, Engineering Electromagnetics, 7th Edition, Tata McGraw-Hill, 2009.

Reference Books:

- 1. Matthew N O Sadiku, Elements of Electromagnetics, 4th edition, Oxford University Press, 2007.
- 2. Edward C. Jordan and Keith G Balmain, Electromagnetic Waves and Radiating Systems, 2nd edition, Prentice Hall of India, 2002.
- 3. John Krauss and Daniel A. Fleisch, Electromagnetics with Applications, 5th edition, Tata McGraw Hill, 1999.

MOOCs

https://nptel.ac.in/noc/courses/noc18/SEM1/noc18-ee04 https://www.edx.org/course/electricity-and-magnetism-maxwells-equations https://www.coursera.org/lecture/electrodynamics-introduction/1-1-introduction-to-electromagnetism-qilQb

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1



Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	_	-	-	-	-	1	-
CO2	3	2	2	-	-	-	-	ı	ı	-	-	_	1	-
CO3	3	2	2	-	-	-	-	-	-	-	-	-	1	-
CO4	3	2	2	-	-	-	-	-	•	-	-	-	1	-
CO5	3	2	2	-	_	-	_	-	-	-	-	_	1	-
Average	3	2	2	-	-	-	-	-	-	-	-	-	1	-

Low -1: Medium -2: High-3



SEMESTER – V Program Electives-1

Course: Operating Systems

Course Code	22ECE551	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites:

Course Learning Objectives: Students will be taught;

CLO1	Concepts of operating system and multi programming.				
CLO2	Process management and File structures.				
CLO3	Scheme of memory management.				
CLO4	Resource allocation policies for deadlock prevention or deadlock avoidance.				
CLO5	Security and various attacks.				

Content	No. of Hours / RBT levels
Module-1	8 Hours
Introduction and overview of operating system: Abstract views of an	L2, L3
Operating system, Computing environment and nature of	
computations Classes of operating systems, Batch processing system,	
Multi programming systems, Time sharing systems, Real time	
operating systems, distributed operating systems, modern operating	
system, Virtual machine operating systems, kernel-based operating	
systems, microkernel-based operating systems. (Text-1: 1.1, 3.1, 3.4,	
3.5, 3.6, 3.7, 3.8, 3.9, 4.5, 4.6 & 4.7)	
Module-2	8 Hours
Process Management: Processes and Program, implementing	L2, L3
processes, race conditions, critical sections, control synchronization	
and indivisible operations, synchronization approaches, semaphores.	
(Text-1: 5.1, 5.2, 6.2, 6.3, 6.4, 6.5 & 6.9).	
File systems : Files, Directories, File System Implementation. (Text-2:	
4.1, 4.2, 4.3.1, 4.3.2, 4.3.3 & 4.3.4). Module-3	O Hours
	8 Hours
Memory Management: Static and Dynamic memory allocation, Memory allocation to a process, Reuse of memory, Contiguous	L2, L3
memory allocation, Non-contiguous memory allocation, Paging,	
Segmentation, segmentation with paging. (Text-1: 11.2, 11.4, 11.5.1,	
11.6, 11.7, 11.8, 11.9 & 11.10).	
Module-4	8 Hours
Deadlocks: Resources, Introduction to Deadlocks, The ostrich	L2, L3
algorithm, Deadlock detection and recovery, Deadlock avoidance,	,
Deadlock prevention. (Text-2: 6.1, 6.2, 6.3, 6.4, 6.5 & 6.6).	

Module-5	
Security and Protection: overview of security and protection,	
security attacks, formal aspects of security, Encryption,	8 Hours
authentication and password security, protection structures,	L2, L3
capabilities, classification of computer security, case studies in	
security and protection. (Text-1: 15.1, 15.2, 15.3, 15.4, 15.5, 15.6,	
15.7, 15.8 & 15.9).	

CO1	Explain the various classes, structure of operating system and multi						
CO2	Describe the File systems and process requirement in an operating system.						
CO3	Analyze the management allocation schemes and segmentation.						
CO4	Describes the resource allocation policies to prevent the deadlock.						
CO5	Apply the knowledge of operating system for security and protection.						

Textbooks:

- 1. Dhamdhere, Operating Systems A concept based approach, TMH, 3rd edition.
- 2. Andrew S Tanenbaum, Herbert Boss, "Modern Operating Systems", 4th edition.

Reference Books:

- 1. Operating Systems Concepts, Silberschatz and Galvin, John Wiley, 7th Edition, 2001.
- 2. Operating System Internals and Design Systems, William Stalling, Pearson Education, 4th Ed, 2006

MOOCs

https://nptel.ac.in/courses/106106144 https://www.coursera.org/specializations/codio-introduction-operating-systems

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1



Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1									2	2	1
CO2	3	2	1									2	2	1
CO3	3	2	1									2	2	1
CO4	3	2	1									2	2	1
CO5	3	2	1									2	2	1
Average	3	2	1									2	2	1

Low -1: Medium -2: High-3



SEMESTER – V Program Electives-1

Course: Nanoelectronics

Course Code	22ECE552	CIE Marks	50
Hours/Week (L: T: P)	3: 0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Fundamentals of Physics and Chemistry, Solid State Devices.

Course Learning Objectives: Students will be taught;

	<u> </u>
CLO1	Development in Nano electronics, structure and properties
CLO2	Characterization and Inorganic semiconductor nanostructures
CLO3	Fabrication techniques
CLO4	Carbon Nanostructures and nanotubes
CLO5	Nanosensors and its applications

Content	No. of Hours / RBT levels
Module-1	8 Hours
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nano meter length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of Nano systems (Text 1: 1.1, 1.2, 1.3 & 1.4)	L3
Module-2	8 Hours
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques. Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text 1: 2.1, 2.2, 2.4, 2.5, 2.6, 3.1, 3.2, 3.3 & 3.4)	L3
Module-3	8 Hours
Fabrication techniques: Requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. Physical processes: Modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, inter band absorption, intraband absorption, Light emission processes, phonon	L3

bottleneck, quantum confined stark effect, nonlinear effects, coherence	l
and dephasing, characterization of semiconductor nanostructures: optical	l
electrical and structural (Text 1: 3.5, 3.6 & 3.7)	l
Module-4	8 Hours
Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon	L3
Nanotubes, application of Carbon Nanotubes. (Text 2: 5.1)	l
Module-5	8 Hours
Nanosensors: Introduction, What is Sensor and Nano sensors? What	L3
makes them Possible? Order from Chaos, Characterization, Perception,	l
Nanosensors Based On Quantum Size Effects, Electrochemical Sensors,	l
Sensors Based On Physical Properties, Nanobiosensors, Smart dust Sensor	l
for the future. (Text 3: 12.1 to 12.10)	l
Applications: Injection lasers, quantum cascade lasers, single-photon	l
sources, biological tagging, optical memories, coulomb blockade devices,	l
photonic structures, QWIP 's, NEMS, MEMS (Text 1: 3.8 till	l
3.8.5,3.8.7,3.8.8	1

CO1	Explain the basic principles behind Nano electronics and the process flow required
	to fabricate state-of-the-art transistor technology.
CO2	Describe the particles size on mechanical, thermal, optical and electrical properties
	of nanomaterials.
CO3	Explicate the fabrication techniques and physical process
CO4	Explain the properties used for sensing and the use of smart dust sensors.
CO5	Assess the various sensors to prepare and characterize nanomaterials

Textbooks:

- 1. Ed Robert Kelsall, Ian Hamley and Mark Geoghegan, Nanoscale Science and Technology, John Wiley Sons Ltd, 2007.
- 2. Charles P Poole, Jr and Frank J Owens, Introduction to Nanotechnology, Wiley India (P) Ltd, Reprint 2012
- 3. T Pradeep, Nano: The Essentials-Understanding Nanoscience and Nanotechnology, 13th reprint, McGraw Hill Education (India) Private Limited, 2016.

Reference Books:

1. Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski and Gerald J Iafrate, Hand Book of Nanoscience Engineering and Technology, CRC press, 2012.

MOOCs:

https://www.youtube.com/watch?v=wdNFCWLuC10 https://www.youtube.com/watch?v=2voX3fjMGjA https://www.youtube.com/watch?v=nnq5asbB_Ow

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs) and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
CO/PO	P01	P02	PO3	P04	PO5	P06	P07	P08	P09	PO10	P011	P012	PS01	PS02
CO1	3	3	2									1	3	1
CO2	3	3	2									1	3	1
CO3	3	3	2									1	3	1
CO4	3	3	2									1	3	1
CO5	3	3	2									1	3	1
Average	3	3	2									1	3	1

Low-1: Medium-2: High-3



SEMESTER –V Program Electives-1

Course: Power Electronics

Course Code	20ECE553	CIE Marks	50
Hours/Week (L: T: P)	3: 0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Elements of Electrical Engineering and Electronics Engineering and Analog Electronic Circuits.

Course Learning Objectives: Students will be taught;

CLO1	Power devices and its characteristics
CLO2	Thyristor circuits for turn on, turn off and controlled rectification.
CLO3	Controlled Rectifiers ,AC voltage controllers
CLO4	Choppers, Thyristors turn off methods
CLO5	Inverters, Voltage control and Pulse width Modulated Inverters.

Module-1 Introduction: Applications of power electronics, Types of power electronics circuits, Peripheral effects, Power semiconductor devices. Text-1: 1.1,1.3,1.6 &1.8) Power Transistor: Power BJT's, switching characteristics, switching limits, Base derive control, Power MOSFET's, switching characteristics, IGBT's, solation of gate and base drives. (Text-1: 4.6.2, 4.6.3, 4.16, 4.3.2, 4.7.1 & 1.17) Module-2 Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	8 Hours L3
Plectronics circuits, Peripheral effects, Power semiconductor devices. Text-1: 1.1,1.3,1.6 &1.8) Power Transistor: Power BJT's, switching characteristics, switching limits, Base derive control, Power MOSFET's, switching characteristics, IGBT's, solation of gate and base drives. (Text-1: 4.6.2, 4.6.3, 4.16, 4.3.2, 4.7.1 & 1.17) Module-2 Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	13
Power Transistor: Power BJT's, switching characteristics, switching limits, Base derive control, Power MOSFET's, switching characteristics, IGBT's, solation of gate and base drives. (Text-1: 4.6.2, 4.6.3, 4.16, 4.3.2, 4.7.1 & 4.17) Module-2 Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	LJ
Power Transistor: Power BJT's, switching characteristics, switching limits, Base derive control, Power MOSFET's, switching characteristics, IGBT's, solation of gate and base drives. (Text-1: 4.6.2, 4.6.3, 4.16, 4.3.2, 4.7.1 & 1.17) Module-2 Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	
Rase derive control, Power MOSFET's, switching characteristics, IGBT's, solation of gate and base drives. (Text-1: 4.6.2, 4.6.3, 4.16, 4.3.2, 4.7.1 & 4.17) Module-2 Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	
Module-2 Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, Darallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	
Module-2 Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	
Module-2 Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	
Thyristors: Introduction, Thyristor characteristics, two transistor model of Thyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	
Chyristor. Turn-on Methods of a Thyristor, Dynamic turn-on Switching Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	8 Hours
Characteristics, Turn-off Mechanism, series operation of Thyristor, parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	L3
parallel operation of Thyristor, di / dt and dv / dt protection, Thyristor	
iring circuits, UniJunction Transistor, Comparison between Transistors	
and Thyristors (Text-1:9.1,9.2,9.3,9.4,9.7,9.8,9.9,9.10,9.13,9.14, Text-	
2:2.8,2.9,2.13)	
Module-3	8 Hours
Controlled Rectifiers: Introduction, Single Phase Full Converters, Single Phase Dual Converters (Text-1: 10.1,10.2,10.3)	L3
AC Voltage Controllers: Introduction, Performance Parameters of AC	
/oltage Controllers, Single –Phase Full –wave controllers with resistive	
oads, Single –Phase Full –wave controllers with Inductive Loads.(Text-1:	
1.1, 11.2, 11.3 &11.4)	
Module-4	8 Hours
Choppers: Introduction, Basic Chopper Classification, Basic Chopper	L3
Operation, Control Strategies, Chopper Configuration. Thyristor Chopper	
Circuits, Jones Chopper, Morgan Choppers, A.C. Choppers (Text-2: 8.1-	
3.10)	
Furn-off Methods: Natural Commutation, Forced Commutation(Text-2: 2.10)	

Module-5	8 Hours
Inverters : Introduction, classification of Inverters, Single-Phase Half-	L3
Bridge Voltage-Source Inverters, Single-Phase Full-Bridge Inverters,	
Performance Parameters of Inverters, Voltage Control of Single-Phase	
Inverters, Pulse Width Modulated(PWM)Inverters (Text-2: 9.1 to 9.7)	

CO1	Describe the characteristics of different power devices and identify the
COI	applications associated with them.
CO2	Determine the brief description of Thyristor Circuits.
CO3	Explain the principle operation of controlled Rectifiers and AC Voltage Controllers.
CO4	Describe the working principle of choppers in D.C to D.C conversion.
CO5	Illustrate the working of inverter circuits with R and RL Loads, Voltage control and
005	Pulse width Modulated Inverters.

Textbooks:

- 1. Mohammad H Rashid, Power Electronics Circuits, Devices and Applications, 4th Edition, Pearson Education Inc, 2014.
- 2. M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, McGraw Hill Education (India)Private Limited, 2013

Reference Books:

- 1. Dr. P. S. Bimbhra, Power Electronics, 3rd Edition, Khanna Publishers, 2012.
- 2. P.C. Sen, Power Electronics, 18th reprint, Tata McGraw Hill Publishing Company Limited, 2002.

MOOCs:

https://www.youtube.com/watch?v=JV-Dw_caz3k https://www.youtube.com/watch?v=sMnuBfwHsQw https://www.youtube.com/watch?v=wMABx9TFVIw

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1



Table 1: Distribution of weightage for CIE & SEE of Regular courses.

	<u> </u>		
	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

					CC)-PO a	nd PSC) Map	ping					
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	-	-	-	-	-	-	-	-	-	3	1
CO2	3	2	2	-	-	-	-	-	-	-	-	-	3	1
CO3	3	2	2	-	-	ı	-	ı	ı	-	ı	-	3	1
CO4	3	2	2	-	-	1	-	1	1	-	ı	-	3	1
CO5	3	2	2	-	-	ı	-	ı	ı	-	ı	-	3	1
Average	3	2	2	-	-	-	-	-	-	-	-	-	3	1

Low-1: Medium-2: High-3



SEMESTER – V Program Electives-1

Course: Satellite Communication

Course Code	22ECE554	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Satellite Orbits and Trajectories.
CLO2	Satellite subsystem and Earth Station.
CLO3	Multiple Access Techniques and Satellite Link Design Fundamentals.
CLO4	Communication Satellites.
CLO5	Remote Sensing Satellites, Weather Forecasting Satellites and Navigation Satellites.

Content	No. of Hours / RBT levels
Module 1	8 Hours
Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital	L2
parameters, Injection velocity and satellite trajectory, Types of Satellite	
orbits, Orbital perturbations, Satellite stabilization, Orbital effects on	
satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation	
angle. (Text 1: 2.1, 2.2, 2.3, 3.3, 3.4, 3.5, 3.6, 3.7.1 & 3.7.2)	
Module 2	8 Hours
Satellite subsystem: Power supply subsystem, Attitude and Orbit control,	L2
Tracking, Telemetry and command subsystem, Payload.	
Earth Station: Types of earth station, Architecture, Design considerations,	
Testing, Earth station Hardware, Satellite tracking. (Text1: 4.1, 4.5, 4.6,	
4.7, 4.8, 8.1, 8.2, 8.3, 8.4, 8.5 & 8.6)	
Module 3	8 Hours
Multiple Access Techniques: Introduction, FDMA, SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA.	L3
Satellite Link Design Fundamentals: Transmission Equation, Satellite Link	
Parameters, Propagation considerations.(Text1: 6.1, 6.2, 6.3, 6.4, 6.13,	
6.14, 7.1, 7.2 &7.4).	
Module 4	8 Hours
Communication Satellites: Introduction, Related Applications, Frequency	L2
Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony,	
Satellite Television, Satellite radio, Regional satellite Systems, National	
Satellite Systems.(Text1: 9.1, 9.3, 9.5, 9.6, 9.7, 9.8, 9.10.2 & 9.10.3).	



Module 5	8 Hours
Remote Sensing Satellites: Classification of remote sensing systems,	L3
orbits, Payloads, Types of images: Image Classification, Interpretation,	
Applications.	
Weather Forecasting Satellites: Fundamentals, Images, Orbits, Payloads,	
Applications.	
Navigation Satellites: Development of Satellite Navigation Systems, GPS	
system, Applications.(Text1: 10.1, 10.2, 10.7, 10.8, 10.9, 10.10, 11.1, 11.3,	
12.1, 12.2 & 12.8).	

CO1	Comprehend the satellite orbits and its trajectories with the definitions of parameters
COI	associated with it.
CO2	Describe the electronic hardware systems associated with the satellite subsystem and
CO2	earth station.
CO3	Compute the satellite link parameters under various propagation conditions with the
CO3	illustration of multiple access techniques.
CO4	Discuss different types of communication satellites.
CO5	Explain the satellites used as remote sensing, weather forecasting and Navigational
COS	satellites.

Textbooks:

1.Anil K. Maini, Varsha Agrawal, Satellite Communications, 1st edition, Wiley India Pvt. Ltd., 2015.

Reference Books:

- 1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International,2006.
- 2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1



Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

					CC)-PO a	nd PSC) Мар	ping					
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	ı	-	-	ı	1	1	3	ı	-	ı	1	2	2
CO2	2	2	2	2	-	1	1	-	-	1	-	1	2	1
CO3	1	2	-	1	ı	1	ı	1	ı	-	-	-	1	1
CO4	1	2	2	1	ı	1	ı	1	ı	1	ı	1	2	1
CO5	-	. 1	-	-	1	2	1	1	-	-	_	-	3	1
Average	2	2	2	1	-	1	1	2	-	1	-	1	2	1

Low-1: Medium-2: High-3



SEMESTER -V

Course: Programming in JAVA

Course Code	22ECE56	CIE Marks	50
Hours/Week (L: T: P)	2:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Features of object-oriented programing.
CLO2	Set up Java JDK environment to create, debug and run simple Java programs
CLO3	Learn object oriented concepts using programming examples
CLO4	Create multi-threaded programs and event handling mechanism
CLO5	Introduce event driven Graphical User Interface(GUI) programming using swings

Content	No. of Hours/ RBT levels
Module-1	8 Hours
Introduction to JAVA: Java's magic: the Byte code; Java Development Kit	L2
(JDK); the Java Buzzwords, Object-oriented programming; Simple Java	
programs. Data types, variables and arrays, Operators, Control Statements.	
Classes & Objects: Classes fundamentals; Declaring objects; Constructors,	
this keyword, garbage collection.	
Module-2	8 Hours
Inheritance: inheritance basics, using super, creating multi-level hierarchy,	L3
method overriding, Abstract class	
Exception handling: Exception-Handling Fundamentals, Exception Types,	
Uncaught Exceptions, using try and catch, Multiple catch Clauses, Nested try	
Statements, throw, throws, finally, Java's Built-in Exceptions, Creating Your	
Own Exception Subclasses, Chained Exceptions, Using Exceptions	
Module-3	8 Hours
Packages and Interfaces: Packages, Access Protection, Importing Packages, Interfaces.	L3
Multi-Threaded Programming: What are threads? How to make the classes	
threadable; Extending threads; Implementing runnable; Synchronization;	
Changing state of the thread; Bounded buffer problems, producer consumer	
problems.	
Module-4	8 Hours
Event Handling: Two event handling mechanisms; The delegation event	L3
model; Event classes; Sources of events; Event listener interfaces; Using the	
delegation event model; Adapter classes; Inner classes.	
Module-5	8 Hours
Swings: Swings: The origins of Swing; Two key Swing features; Components	L2
and Containers; The Swing Packages; A simple Swing Application; Create a	
Swing Applet; Jlabel and Imagelcon; JTextField;The Swing Buttons; JTabbedpane; JScrollPane; JList; JComboBox; JTable.	

CO1	Describe the basic concepts of object-oriented programming language.
CO2	Develop java programs to illustrate the concept of inheritance and exception handling.
CO3	Apply Multi-threading concepts to create parallel programming.
CO4	Analyze Event Handling mechanisms to create interactive programs.
CO5	Develop GUI interfaces for a computer program to interact with users using Swings.

Textbooks:

- 1. Herbert Schildt, Java The Complete Reference, 7th Edition, Tata McGraw Hill, 2007 **Reference Books:**
- 1. Mahesh Bhave and Sunil Patekar, "Programming with Java", First Edition, Pearson Education, 2008, ISBN:9788131720806
- 2. Rajkumar Buyya, S Thamarasi selvi, xingchen chu, Object oriented Programming with java, Tata McGraw Hill education private limited.
- 3. E Balagurusamy, Programming with Java A primer, Tata McGraw Hill companies.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
			Marks
	CIE Test-1	40	
	CIE Test-2	40	
CIE	CIE Test-3	40	50
	Quiz 1/AAT	05	
	Quiz 2/AAT	05	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
СО	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	-	-	-	-	-	-	-	-	-	1	-
CO2	3	3	3	-	-	-	1	-	1	-	-	-	1	-
CO3	3	3	3	-	-	-	1	-	1	-	-	-	1	-
CO4	3	3	3	-	-	-	-	-	-	-	-	-	1	-
CO5	3	3	3	-	-	-	-	-	-	-	-	-	1	-
Average	3	3	3	-	-	-	-	-	-	-	-	-	1	-

Low-1: Medium-2: High-3



SEMESTER - V/VI

Course: Environmental Science

Subject Code	22CIV57/66	CIE Marks	50
Hours/Week (L: T: P)	1:0:0	SEE Marks	50
No. of Credits	1	Examination Hours	1 hour

Course Learning Objectives: Students will be taught;

CLO1	The fundamentals of environmental science.
CLO2	The types of natural resources
CLO3	The various global environmental concerns.
CLO4	The types of wastes generated and their handling at a basic level
CLO5	The area of environmental law and policies with a few important acts in the field

	No. of
Content	Hours/
	RBT Levels
Module 1	04 Hours /
Environment:	L2
Definition, scope & importance	
• Components of Environment Ecosystem: Structure and function of various	
types of ecosystems	
Human Activities – Food, Shelter, and Economic & Social Security.	
• Population - Growth, variation among nations - population explosion and	
impact on environment	
Biodiversity: Types, Value, Hot spots, Threats and Conservation of biodiversity,	
Forest Wealth, and Deforestation.	
Module 2	04 Hours /
Natural Resources: Forest, Water, Mineral, Food, Energy, Land Environmental	L2
Pollution - Definition - causes, effects and control measures of: (a) Air pollution	
(b) Water pollution (c) Soil pollution (d) Marine pollution (e) Noise pollution (f)	
Thermal pollution (g) Nuclear hazards.	
Module 3	04 Hours /
Global Environmental Concerns (Concept, policies and case-studies): Ground	L2
water depletion/recharging, Climate Change; Acid Rain; Ozone Depletion; Radon	
and Fluoride problem in drinking water; Resettlement and rehabilitation of	
people, Environmental Toxicology.	
Module 4	04 Hours /
Sources: Sources of Solid waste, Types of solid waste, Physical and Chemical	L2
composition of municipal solid waste. Solid Waste Management Rules in India,	
Sources and management of E – Waste, Biomedical Waste, Hazardous waste, and	
construction waste at individual and community level.	
Socio-economic aspect of waste management Environmental Toxicology.	

Module 5					
Latest Developments in Environmental Pollution Mitigation Tools (Concept and	L2				
Applications): Environment Impact Assessment, Environmental Management					
Systems, ISO14001; Environmental Stewardship, NGOs.					

C01	Understand holistically the key concepts "Environment", and "Biodiversity".
CO2	Classify the types of natural resources available and the effects of anthropogenic interventions.
C03	Express the gravity of various global environmental concerns.
CO4	Categorize the types of wastes generated and their handling at a basic level.
CO5	Understand the importance of environmental law and policies.

Textbooks:

- 1. Environmental studies, Benny Joseph, Tata Mcgraw-Hill 2nd edition 2012
- 2. Environmental studies, S M Prakash, pristine publishing house, Mangalore 3rd edition-2018
- 3. Gilbert M.Masters, Introduction to Environmental Engineering and Science, 2nd edition, Pearson Education, 2004

Reference books:

- 1. Benny Joseph, Environmental studies, Tata Mcgraw-Hill 2nd edition 2009
- 2. M.Ayi Reddy, Textbook of Environmental Science and Technology, BS publications
- 3. 2007 Dr. B.S Chauhan, Environmental Studies, University of science press 1st edition

Web References:

https://www.hzu.edu.in/bed/E%20V%20S.pdf

https://onlinecourses.nptel.ac.in/noc23_hs155/preview

https://onlinecourses.swayam2.ac.in/cec19_bt03/preview

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 50 marks with multiple choice questions of 1 mark each covering all aspects of the syllabus.

Continuous Internal Evaluation (CIE): Three Tests are to be conducted for 50 marks each. The average of the three tests are taken for computation of CIE. Question paper for each of the CIE is to be of the multiple-choice type with 50 question each.

Typical Evaluation pattern for regular courses is shown in Table.

Table 1: Distribution of weightage for CIE & SEE for 1 credit course

	Component	Marks	Total Marks			
	CIE Test-1	50				
CIE	CIE Test-2	50	50			
	CIE Test-2	50				
SEE	Semester End Examination	50	50			
	Grand Total					

	CO/PO Mapping														
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1	PO11	PO12	PSO1	PSO2	PSO3
										0					
CO1	2	-	-	-	-	-	3	-	-	-	-	-	1	-	-
CO2	2	1	-	-	-	-	3	-	-	-	-	1	1	-	1
CO3	2	-	2	-	-	2	3	1	-	-	-	1	1	-	1
CO4	2	2	-	-	-	2	3	-	-	-	-	-	-	-	1
CO5	2	-	-	-	-	2	3	-	-	-	-	-	-	1	1
Average	2	1.5	2	-	-	2	3	1	-	-	-	1	1	1	1

Low-1: Medium-2: High-3



SEMESTER - V/VI

Course: Universal Human Values

Subject Code	22UHV57/66	CIE Marks	5
			0
Hours/Week (L: T: P)	1:0:0	SEE Marks	5
			0
No. of Credits	1	Examination Hours	1 hour

Course Learning Objectives: Students will be taught;

CLO1	To create an awareness on Engineering Ethics and Human Values.
CLO2	To understand social responsibility of an engineer.
CLO3	To appreciate ethical dilemma while discharging duties in professional life.

Content	No. of	
	Hours	
Module 1	05	
Introduction to Value Education		
Value Education, Definition, Concept and Need for Value Education.	Hours	
The Content and Process of Value Education.		
Basic Guidelines for Value Education,		
Self-exploration as a means of Value Education.		
Happiness and Prosperity as parts of Value Education.		
Module 2	05	
Harmony in the Human Being		
Human Being is more than just the Body.		
Harmony of the Self ('I') with the Body.		
Understanding Myself as Co-existence of the Self and the Body.		
Understanding Needs of the Self and the needs of the Body.		
Understanding the activities in the Self and the activities in the Body.		
Module 3	05 Hours	
Harmony in the Family and Society and Harmony in the Nature		
• Family as a basic unit of Human Interaction and Values in Relationships.		
The Basics for Respect and today's Crisis: Affection, Guidance,		
Reverence, Glory, Gratitude and Love,		
Comprehensive Human Goal: The Five Dimensions of Human Endeavour.		
Harmony in Nature: The Four Orders in Nature.		
The Holistic Perception of Harmony in Existence.		
Module 4	05	
Social Ethics		
The Basics for Ethical Human Conduct, Defects in Ethical Human		
Conduct.		
Holistic Alternative and Universal Order,		
Universal Human Order and Ethical Conduct.		
Human Rights violation and Social Disparities.		

Module 5	05
Professional Ethics	Hours
 Value based Life and Profession., Professional Ethics and Right 	
Understanding.	
Competence in Professional Ethics.	
 Issues in Professional Ethics – The Current Scenario. 	
Vision for Holistic Technologies	
Production System and Management Models.	

CO1	Understand the significance of value inputs in a classroom and start applying them intheir life and profession
CO2	Distinguish between values and skills, happiness and accumulation of physical facilities, the Self and the Body, Intention and Competence of an individual, etc.
CO3	Understand the role of a human being in ensuring harmony in society and nature.
CO4	Distinguish between ethical and unethical practices and start working out the strategy toactualize a harmonious environment wherever they work.

Textbooks:

- 1. A.N Tripathy, Human Values, New Age International Publishers, 2003.
- 2. Bajpai. B. L, Indian Ethos and Modern Management, New Royal Book Co, Lucknow, 2004
- 3. Bertrand Russe II, Human Society in Ethics & Politics

Reference books:

- 1. Corliss Lamont, Philosophy of Humanism.
- 2. Gaur. R.R., Sangal. R, Bagari G.P, A Foundation Course in Value Education, Excel Books, 2009.
- 3. I.C. Sharma, Ethical Philosophy of India, Nagin & co, Julundhar
- 4. William Lilly- Introduction to Ethics -Allied Publisher

Scheme of Examination:

Semester End Examination (SEE): SEE Question paper is to be set for 50 marks with multiple choice questions of 1 mark each covering all aspects of the syllabus.

Continuous Internal Evaluation (CIE): Three Tests are to be conducted for 50 marks each. The average of the three tests are taken for computation of CIE. Question paper for each of the CIE is to be of the multiple-choice type with 50 question each. Typical Evaluation pattern for regular courses is shown in Table.

Table 1: Distribution of weightage for CIE & SEE for 1 credit course

	Component	Marks	Total Marks
	CIE Test-1	50	
CIE	CIE Test-2	50	50
	CIE Test-3	50	
SEE	Semester End Examination	50	50
	Grand Total		100



	CO/PO Mapping															
CO/PO	PO1	PO2	PO3	PO4	PO5	P06	P07	P08	P09	PO10	PO11	PO12	PS01	PS02	PS03	PS04
CO1	ı	-	ı	-	-	ı	-	2	ı	-	-	1	-	ï	-	-
CO2	ı	ı	Í	-	ı	ı	-	2	ı	-	-	1	-	Í	-	ı
CO3	-	1	-	-	1	ı	-	2	ı	-	-	1	-	-	-	ı
CO4	ı	-	ı	-	-	ı	-	2	ı	-	-	1	-	ï	-	-
Average	-	-	=	-	-	-	-	2	-	-	-	1	-	-	-	-

SEMESTER – V

Course: Digital Signal Processing Laboratory

Course Code	22ECEL58	CIE Marks	50
Hours/Week (L:T:P)	0:0:2	SEE Marks	50
No. of Credits	1	Examination Hours	03

Course Learning Objectives: Student will be taught;

CLO1	Generate standard test signals and verify Sampling Theorem.
CLO2	DFT of a discrete signal and verify its properties.
CLO3	Difference equation and compute convolution & correlation.
CLO4	Implement digital filters.
CLO5	Perform computations using DSP hardware.

SI. No.	Content	RBT levels
Li	st of Experiments to be conducted using Hardware Components/Simu	lation Tools
	PARTA: Experiments Using MATLAB	
1.	Write a MATLAB program to verify Sampling Theorem for different conditions.	L3
2.	Write a MATLAB program to perform Linear and Circular Convolution of two given sequences.	L3
3.	Write a MATLAB program to perform Auto and Cross Correlation of two sequences and verification of their properties.	L3
4.	Write a MATLAB program to Solve a given difference equation to find step and steady state responses.	L3
5.	Write a MATLAB program to Compute N point DFT of a given sequence and plot magnitude and phase spectrum.	L3
6.	Write a MATLAB program to i) Verify DFT properties (Linearity and Parseval's Theorem). ii) Compute DFT of Square pulse and Sinc function.	L3
7.	Write a MATLAB program to Design and implement Low pass FIR filter for the given specifications: Normalized cutoff frequency = 0.48 Order of the filter = 34	L3
8.	Write a MATLAB program to Design and implement digital Low Pass IIR filter to meet given specifications: Passband edge frequency = 2000Hz Stopband edge frequency = 3000Hz Passband attenuation = - 3dB Stopband attenuation = - 15dB Sampling frequency = 8000 samples/sec	L3

	PART-B: Experiments Using DSP Starter Kit					
9.	Write a C program to Generate Sine Wave and Standard Test Signals using DSP starter kit.	L3				
10.	Write a C program to Compute Linear Convolution of two sequences using DSP starter kit.	L3				
11.	Write a C program to Compute the N- point DFT of a given sequence using DSP starter kit.	L3				
12.	Write a C program to Determine the impulse response of second order system using DSP starter kit.	L3				

	,				
CO1	Apply sampling theorem to verify different conditions of sampling.				
CO2	Obtain output response of the system using Linear Convolution, circular				
	convolution, autocorrelation and cross correlation of the sequences.				
CO3	Determine FFT of given sequence and verify its properties.				
CO4	Design and implement the digital FIR/IIR filter for the specifications of Passband				
	edge frequency, Stopband edge frequency, sampling frequency and attenuation.				
CO5	Determine the output response of the system using DSP Processor.				

Scheme of Examination:

Semester End Examination (SEE):

All laboratory experiments are to be included for practical examination. Students can pick one experiment from the questions lot prepared by the examiners. Change of experiment is allowed only once and 15% Marks allotted to the write up part to be made zero.

	Semester End Examination Evaluation				
SL.NO	ACTIVITY	MARKS			
1	Write-Up	15			
2	Conduction	70			
3	Viva Voce	15			
	TOTAL	100			

Note: The marks scored will be proportionately reduced to 50

Continuous Internal Evaluation (CIE):

As part of CIE process, progressive continuous evaluation is done for laboratory work on weekly basis of conduct of experiment by student either individually or in group based on the laboratory. The breakup of the marks allocated is given in the TABLE-1

	indicatory. The predicap of the marks discourse is given in the marks a			
	TABLE-1 WEEKLY EVALUATION OF CONDUCT OF EXPERIMENT			
SL.NO	ACTIVITY	MAX MARKS		
1	Conduct of experiment and documentation	10		
2	Analysis & interpretation of results	5		
3	Viva voce	5		
	TOTAL	20		

Internal examination is conducted at the end of the semester or on completion of a predefined set of experiments based on the laboratory. The evaluation detail of the laboratory internal exam is given in TABLE-2



	TABLE-2 LAB INTERNAL EXAMINATION				
SL.NO	ACTIVITY	MAX MARKS			
1	Detailed write-up about the experiment with relevant procedure and calculation.	5			
2	Conduction of experiment	20			
3	Viva voce	5			
	TOTAL				

	TABLE-3 FINAL CIE CALCULATION				
SL.NO	METRICS USED	MAX MARKS			
1	Average of all weekly evaluations of conduct of an experiment	20			
2	Lab Internal Examination	30			
	TOTAL	50			

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2			1			2	1			1	1	1
CO2	3	2			1			2	1			1	1	1
CO3	3	2			1			2	1			1	1	1
CO4	3	2			1			2	1			1	1	1
CO5	3	2			1			2	1			1	1	1
Average	3	2			1			2	1			1	1	1



SEMESTER - VI

Course: Information Theory and Coding

Course Code	22ECE61	CIE Marks	50
Hours/Week (L:T:P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Communication systems

Course Learning Objectives: Students will be taught;

CLO1	Information content and its measurement of both independent and dependent
	sources
CLO2	Source encoding algorithms and its properties
CLO3	Communication channel and different Entropies associated with channels
CLO4	Error control coding
CL05	Convolution encoding algorithm for error detection and correction.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Information Theory: Introduction, Measure of information, Information	L3
content of message, Average Information content of symbols in Long	
Independent sequences, Average Information content of symbols in Long	
dependent sequences, Markov Statistical Model for Information Sources,	
Entropy and Information rate of Markoff Sources, Extension of Discrete	
memoryless source. (Text 1)	
Module-2	8 Hours
Source Coding: Encoding of the Source Output, Shannon's Encoding	L3
algorithm, Shannon Fano algorithm, Huffman coding, Source coding	
theorem, prefix codes, Kraft McMillan Inequality properties (KMI)	
,Arithmetic Coding, Lempel – Ziv Algorithm. (Text 1)	
Module-3	8 Hours
Information Channels: Communication Channels, Discrete Communication	L3
channels, Channel Matrix, Joint Probability Matrix (JPM), System Entropies,	
Mutual information, Channel Capacity, Channel capacity of Binary	
Symmetric Channel, Binary Erasure Channel, Capacity calculation using	
Muroga's method,	
Continuous Channels, Shannon Hartley law and its Implications. (Text 1).	
Module-4	8 Hours
Error Control Coding: Introduction, Examples of Error control coding,	L3
methods of Controlling Errors, Types of Errors, types of Codes. Linear Block	
Codes- matrix description of Linear Block Codes, Error detection and	
Correction capabilities of Linear Block Codes, Single error correction	
Hamming code. Binary Cyclic Codes- Algebraic Structure of Cyclic Codes,	
Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error	
Detection and Correction (Text- 1).	
Module-5	8 Hours
Convolution Codes: Convolution Encoder, Time and Transform domain	L3
approach, code tree, Trellis and state diagram, Viterbi Algorithm, BCH and	
Golay codes. (Text-2)	

CO1	Explain concept of Dependent & Independent Source, measure of information,
	Entropy, Rate of Information and Order of a source
CO2	Obtain the code words for the information content using Encoding Algorithms
CO3	Compute system entropies, mutual information and capacity of a Channels.
CO4	Analyze the code words of a k- bit messages using Linear block codes and Cyclic codes.
CO5	Compute the output for the given input sequences using time and transform domain
	approach.

Text Books:

- 1. K. Sam Shanmugam, Digital and Analog communication systems, John Wiley India Pvt. Ltd, 1996.
- 2. Bernard Sklar, Digital communication Fundamentals and Applications, Pearson Education Pvt. Ltd, 2003

Reference Books:

- 1. Simon Haykin, Digital communication, John Wiley India Pvt. Ltd, 2008
- 2. J. Das, S. K. Mullick and P. K. Chatterjee, Principles of Digital Communication, Wiley, 1986
- 3. HariBhat and Ganesh Rao, Information Theory and Coding, Cengage, 2017.
- 4. Todd K Moon, Error Correction Coding, Wiley Std. Edition, 2006

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses.

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	Grand Total		100



	CO-PO and PSO Mapping													
CO/PO	P01	P02	PO3	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PS01	PS02
CO1	3	3	1		-	-	-	ı	-	-		-	-	-
CO2	3	3	ı	-	-	-	-	-	-	-	-	-	2	1
CO3	3	ı	ı	ı	-	-	-	ı	-	-	ı	1	ı	1
CO4	3	3	-	-	_	_	_	1	_	_	-	1	2	-
CO5	3	-	ı	ı	-	-	-	1	-	-	-	1	2	1
Average	3	3	-	-	-	_	-	1	_	-	-	1	2	1

SEMESTER - VI

Course: ARM Controller (Integrated)

Course Code	22ECE62	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	4	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	The requirements of an Embedded system.
CLO2	ARM7 architecture and branching instructions.
CLO3	Programming using ARM and THUMB instruction set.
CLO4	Programming to handle an exception and interrupts.
CLO5	Creating task and scheduling them in real time operating system.

Content	No. of Hours/ RBT levels
Module-1	8 Hours
ARM7 Processor Fundamentals: ARM Architecture, Registers, current	L3
program status register, pipeline, exceptions, interrupts and vector table,	
core extensions. Introduction to ARM Instruction Set: Data Processing	
Instructions, Branch Instructions. (Text- 2: 2.1, 2.2, 2.3, 2.4, 3.1 & 3.2)	
Module-2	8 Hours
Introduction to ARM7 Instruction Set: Load Store Instructions, Software	L3
Interrupt Instruction, Program Status Register Instructions, Loading	
Constants, and Conditional Execution.	
Introduction to the THUMB Instruction set: Thumb register usage, ARM7 –	
Thumb Interworking, other branch instructions, Data Processing Instructions,	
Single register Load -Store Instructions, Multiple register Load Store	
Instructions, Stack Instructions, and Software Interrupt Instruction. (Text-2:	
3.3-3.8 & 4.1-4.8)	
Module-3	8 Hours
Interrupts & Exception Handling in ARM7: Exception Handling Interrupts,	L3
Interrupt handling schemes. The Memory Hierarchy and CACHE Memory,	
CACHE Architecture (Text-2: 9.1, 9.2, 9.3.1-9.3.4, 12.1 & 12.2)	
Module-4	8 Hours
CACHE policy, Flushing and Cleaning CACHE Memory, CACHE Lockdown,	L3
Caches and software performances Protected Regions, Initializing the MPU,	
CACHES and write Buffers (Text-2: 12.3, 12.4, 12.5, 12.6, 12.7, 13.1, 13.2 &	
13.3)	
Module-5	8 Hours
Embedded/Real Time Operating System Concepts: A Task, process and	L3
threads, multiprocessing and Multitasking, Task Scheduling, Task	
Communication. (Text 1)	

	Practical Component of IPC	
SI.	Experiments	RBT levels
	ARM Assembly programming	
1.	Write an assembly language program to evaluate the following	
	i) Data transfer Instructions	L3
	ii) Conditional Instructions	
2.	Write an assembly language program to evaluate the following	
	i) Arithmetic Instructions	L3
	ii) Shift and Rotate instructions	
	Interfacing Programming	
Condu	ct the following experiments on an ARM CORTEX	
Condu	ct the following experiments on an ARM CORTEX M3 evaluation	board using
evalua	tion version of Embedded 'C' & Keil uVision-4 tool/compiler.	,
3.	Write an embedded C program to Display "Hello World" message	L3
	using Internal UART.	LJ
4.	Write an embedded C program to Interface a Stepper motor and	L3
	rotate it in clockwise and anti-clockwise direction.	
5.	Write an embedded C program to Interface a DAC and generate	L3
	Triangular and Square waveforms.	
6.	Write an embedded C program to Interface a 4x4 keyboard and	L2
	display the key code on an LCD.	
7.	Write an embedded C program to Demonstrate the use of an	L3
	external interrupt to toggle an LED On/Off.	
8.	Write an embedded C program to Interface a dc motor and control	L3
	its speed.	LJ
9.	Write an embedded C program to Interface a simple Switch and	L3
	display its status through Relay, Buzzer and LED.	

using a sensor and SPI ADC IC

10. Write an embedded C program to measure Ambient temperature

CO1	Explain the Embedded system and its requirements.
CO2	Describe the ARM7 architecture, data processing and Branching Instruction.
CO3	Write program using ARM and Thumb instruction set.
CO4	Analyze the interrupts and write a program for Exception handling in ARM7.
CO5	Explain the need of real time operating system for embedded system applications.

L3

Textbooks:

- 1. Shibu K V, Introduction to Embedded Systems, 2nd edition, McGraw Hill Education, 2009.
- 2. Andrew N. Sloss, ARM system Developers Guide, Elsevier, 1st edition, 2008.

Reference books:

1. K. V. K. K. Prasad, Embedded Real-Time Systems: Concepts, Design & Programming, Dreamtech Press, 2005.

https://www.gadgetronicx.com/keypad-and-lcd-interfacing-with-arm7/

Scheme of Evaluation: (Integrated courses)

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of four sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question from each module.**

The laboratory assessment would be restricted to only the CIE evaluation.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. The average of the three tests are taken for computation of CIE on a scale of 30, the CIE would also include laboratory evaluation for 20 marks. The laboratory marks of 20 would comprise of 10 marks for regular laboratory assessment to include lab record and observation. 10 marks would be exclusive for laboratory internal assessment test to be conducted at the end of the semester.

Typical Evaluation pattern for integrated courses is shown in the Table-1

Table-1: Distribution of weightage for CIE & SEE of Integrated courses

	Component	Marks	Total Marks
	CIE Test-1	30	
CIE	CIE Test-2	30	F0
CIE	CIE Test-3	30	50
	Laboratory	20	
SEE	Semester End Examination	100	50
		100	

					CC	О-РО а	nd PS0) map	ping					
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	2	2	1	-	2	2	-	-	-	2	2	3	2
CO2	1	1	1	2	2	-	-	-	-	-	-	1	2	2
CO3	1	1	1	2	2	-	-	-	-	-	-	1	2	2
CO4	ı	1	1	2	2	ı	ı	-	ı	-	ı	1	2	2
CO5	-	-	-	1	-	-	-	-	-	-	-	2	2	2
Average	1	1	1	2	2	2	2	_	_	-	2	2	2	2

Low-1: Medium-2: High-3

SEMESTER -VI

Course: VLSI Design

Course Code	22ECE63	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Analog Electronic Circuits and Design and Analysis of Digital Circuits

Course Learning Objectives: Students will be taught;

CLO1	MOS transistor theory and CMOS logic.
CLO2	Fabrication process and MOS circuit design process.
CLO3	Basic circuit concepts and scaling of MOS circuits.
CLO4	Subsystem design process with an illustration.
CLO5	Semiconductor memories, system timings, testing, debugging and verification methods.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Introduction: A Brief History, CMOS Logic, MOS Transistor Theory, Long Channel I-V Characteristics, Non- ideal I-V Effects, DC Transfer Characteristics. (Text 2: 1.1, 1.4, 2.1, 2.2, 2.4 & 2.5).	L2, L3
Module-2	8 Hours
Fabrication: nMOS Fabrication, CMOS Fabrication-P-well process and N-well process. MOS Pasign Processes MOS Layers, Stick Diagrams and NOS Design styles.	L2, L3
MOS Design Processes: MOS Layers, Stick Diagrams: nMOS Design style, CMOS Design style, Design Rules and Layout. (Text 1: 1.7, 1.8.1, 1.8.2, 3.1 to 3.3).	
Module-3	8 Hours
Basic Circuit Concepts : Sheet Resistance, Sheet resistance concept applied to MOS transistors and inverters, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads, Propagation Delays. Scaling of MOS Circuits : Scaling Models & Scaling Factors for Device Parameters. (Text 1: 4.1 to 4.9, 5.1, 5.2).	L2, L3
Module-4	8 Hours
Subsystem Design and Layout: Some Architectural Issues, Switch Logic, Gate (restoring) Logic, A parity generator, Multiplexers (Data selectors), Design of 4-bit shifter. Illustration of the Design Processes: Some observations on the design process, Design of an ALU Subsystem, (Text 1: 6.1 to 6.3, 6.4.1, 6.4.3, 7.2.2, 8.1, 8.3)	L2, L3
Module-5	8 Hours
Memory, Registers and Aspects of system Timing: System Timing Considerations, commonly used Storage/Memory elements (Text 1: 9.1, 9.2).	L2, L3
Testing, Debugging and Verification : Introduction: Logic Verification, Manufacturing Test Principles, Design for testability, Boundary Scan (Text 2: 15.1.1, 15.5, 15.6, 15.7).	

CO1	Demonstrate the concepts of MOS transistor theory, CMOS fabrication flow.
CO2	Analyze MOS Circuit Design Processes, Circuit Characterization and Performance
	Estimation.
CO3	Illustrate the scaling of MOS circuits and know the Subsystem Design Process.
CO4	Design of Combinational and Sequential Circuits.
CO5	Explain the Memory, registers, system timing and testability adapted in VLSI
	Design.

Textbooks:

- 1. Douglas A Pucknell and Kamran Eshaghian, Basic VLSI Design, 3rd Edition, Eastern Economy Edition 2006.
- 2. Neil H. E. Weste, David Harris and Ayan Banerjee, CMOS VLSI Design- A Circuits and Systems Perspective, 4th Edition, Pearson Education 2011.

Reference Books:

- 1. Adel Sedra and K. C. Smith, Microelectronics Circuits Theory and Applications, 7th Edition, Oxford University Press, International Version, 2009.
- 2. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Education (India) Private Limited, 2007.
- **3.** Sung Mo Kang and Yosuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3rd Edition, McGraw Hill Education (India) Private Limited,

MOOCs:

https://www.youtube.com/watch?v=sV2xT-WCSSI https://www.youtube.com/watch?v=faiEVOOCe-s https://www.youtube.com/watch?v=arut8G4Ego0 https://www.youtube.com/watch?v=yyliRphXLq4 https://www.youtube.com/watch?v=egfHY-NOt6Y

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1.

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks			
	CIE Test-1	40				
CIE	CIE Test-2	40	F0			
CIE	CIE Test-3	40	50			
	Assignments	10				
SEE	Semester End Examination	50	50			
	Grand Total					

	CO-PO and PSO Mapping													
CO/PO	P01	P02	P03	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	-	1	-	1	-	-	-	-	2	2	2
CO2	3	3	3	-	1	-	-	-	-	ı	2	2	2	2
CO3	3	3	3	-	1	-	-	-	-	1	2	2	2	2
CO4	3	3	3	-	1	-	-	-	-	-	2	2	2	2
CO5	3	3	3	-	1	-	1	_	-	-	2	2	2	2
Average	3	3	3	-	1	-	1	-	-	ı	2	2	2	2



SEMESTER – VI Program Electives-2

Course: Speech Signal Processing

Course Code	21ECE641	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Speech production mechanism and Acoustic phonetics.
CLO2	Processing speech by representing the information by various analysis methods.
CLO3	Speech and designing filter bank.
CLO4	Homomorphic processing of signals.
CLO5	Concept of speech recognizing system.

Content	No. of Hours/ RBT levels
Module 1	8 Hours
Mechanics of Speech: Speech production: Mechanism of speech	L3
production, Acoustic phonetics - Digital models for speech signals -	
Representations of speech waveform: Sampling speech signals, basics of	
quantization, delta modulation, and Differential PCM (Text 1)	
Module 2	8 Hours
Time Domain Models for Speech Processing: Time dependent processing	L3
of speech, Short time energy and average magnitude, Short time average	
zero crossing rate, Speech vs silence discrimination using energy & zero	
crossings, Pitch period estimation, Short time autocorrelation function,	
Short time average magnitude difference function, Pitch period	
estimation using autocorrelation function. (Text 1)	
Module 3	8 Hours
Frequency Domain Methods for Speech Processing: Short Time Fourier	L3
Analysis: Linear Filtering interpretation, Filter bank summation method,	
Overlap addition method, Design of digital filter banks, Implementation	
using FFT, Spectrographic displays, Pitch detection, Analysis by synthesis,	
Analysis synthesis systems. (Text 1) Module 4	O Hours
Homomorphic Speech Processing: Homomorphic systems for	8 Hours L3
convolution, Complex cepstrum, Mel Frequency Cepstral Coefficients	LS
Pitch detection, Formant estimation, Homomorphic vocoder. (Text 1)	
Module 5	8 Hours
Linear Predictive Coding of Speech: Basic principles of linear predictive	L3
analysis, Solution of LPC equations, Prediction error signal, Frequency	
domain interpretation; Speech Recognition: Introduction, Speech	
recognition, Signal processing and analysis methods, Pattern comparison	
techniques, Isolated digit recognizer. (Text 1)	

CO1	Explain the human speech production mechanism.
CO2	Device an algorithm to differentiate speech and silence, pitch and formants in speech signals.
	speech signals.
CO3	Analyze speech signal using Short Time Fourier transform and designing filter
	bank.
CO4	Describe homomorphic processing of signals.
CO5	Explain Linear prediction of signals and design a simple isolated word recognizer.

Textbooks:

1. L. R. Rabiner and R. W. Schafer, Digital Processing of Speech Signals, Pearson Education (Asia) Pvt. Ltd., 2004.

Reference Books:

- 1. Thomas F. Quatieri, Discrete-time Speech Signal Processing: Principles and Practice, Pearson Education (Singapore) Pvt. Ltd., 2002.
- 2. D. O'Shaughnessy, Speech Communications: Human and Machine, Universities Press, 2001.
- 3. L. R. Rabiner and B. Juang, Fundamentals of Speech Recognition, Pearson Education (Asia) Pvt. Ltd., 2004.
- 4. J. R. Deller, Jr., J. H. L. Hansen and J. G. Proakis, Discrete-Time Processing of Speech Signals, IEEE Press, 2000.

E-Books / Web References:

https://b-ok.asia/book/464474/2e717c

MOOCs:

http://www.digimat.in/nptel/courses/video/117105145/L37.html http://www.digimat.in/nptel/courses/video/117105145/L29.html https://www.digimat.in/nptel/courses/video/117105145/L15.html https://nptel.ac.in/courses/117105145

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2		-	-	-	-	-	-	-	-	2	1
CO2	3	2	2		-	-	-	-	-	-	-	-	2	1
CO3	2	1	-		-	-	-	-	-	-	-	-	-	-
CO4	3	2	2		-	1	-	-	-	-	-	1	1	1
CO5	3	2	2		-	1	-	1	-	-	-	1	2	1
Average	3	2	2		-	-	-	-	-	-	-	1	2	1



SEMESTER -VI Program Electives-2

Course: Digital Image Processing

Course Code	22ECE642	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Fundamentals of digital image Processing.
CLO2	Image transforms used in digital image processing.
CLO3	Image enhancement techniques used in Digital image processing.
CLO4	Image restoration techniques and methods used in digital image processing.
CLO5	Morphological operations used in digital image processing.

Content	No. of Hours/ RBT levels
Module 1	8 Hours
Introduction: What is Digital Image Processing? Origins of Digital Image	L3
Processing, Examples of fields that use Digital image processing,	
Fundamental Steps in Digital Image Processing, Components of an Image	
Processing System, Elements of Visual Perception, Light and Electromagnetic	
Spectrum, Image Sensing and Acquisition. (Text1: 1.1 to 1.5 and 2.1 to 2.3)	
Module 2	8 Hours
Image Sampling and Quantization, Some Basic Relationships Between Pixels,	L3
Some Basic Intensity Transformation Functions, Histogram Processing,	
Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening	
Spatial Filters. (Text1: 2.4, 2.5 and 3.2 to 3.6)	
Module 3	8 Hours
Filtering in the Frequency Domain: Basics of Filtering in the Frequency	L3
Domain, image smoothing using frequency domain filters, Image Sharpening	
Using Frequency Domain Filters, Selective Filtering. (Text1: 4.7 to 4.10)	
Module 4	8 Hours
Image Restoration and Reconstruction: A model of image degradation and	L3
restoration process, Noise models, Restoration in the Presence of Noise Only	
using Spatial Filtering and Frequency Domain Filtering, Linear, Position-	
Invariant degradations, Estimating the Degradation Function, Inverse	
Filtering, Minimum Mean Square Error (Wiener) Filtering, Constrained Least	
Squares Filtering. (Text1: 5.1 to 5.9)	
Module 5	8 Hours
Color Image Processing: Color Fundamentals, Color Models, Pseudo color	L3
Image Processing. (Text1: 6.1 to 6.3)	
Morphological Image Processing: Preliminaries, Erosion and Dilation,	
Opening and Closing. (Text1: 9.1 to 9.3)	

CO1	Explain the fundamental processing steps and components of image processing.							
CO2	Illustrate image digitization, basic relationships between pixels and processing in							
	Spatial domain.							
CO3	Apply image processing techniques in both the frequency domains.							
CO4	Analyze image restoration techniques in both spatial and frequency domains.							
CO5	Explain the concept of colour image processing and morphological image							
	processing.							

Text Book:

- 1. Digital Image Processing- Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010. **Reference Books:**
- 1. S.Jayaraman, S. Esakkirajan and T. Veerakumar, Digital Image Processing Tata McGrawHill 2014.
- 2. A K. Jain, Fundamentals of Digital Image Processing, Pearson 2004.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	Grand Total		100

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	-	-	-	-	-	-	-	-	1	-	-	1	-
CO2	1	1	-	-	-	-	-	-	-	-	-	-	-	1
CO3	3	1	2	-	-	-	-	-	1	-	-	1	1	-
CO4	2	1	1	-	-	-	-	-	-	-	-	-	-	1
CO5	2	-	2	-	-	-	-	-	1	1	-	1	1	-
Average	2	1	2		-	-	-		1	1		1	1	1



SEMESTER –VI Program Electives-2

Course: Micro Electro Mechanical Systems

Course Code	22ECE643	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Basic Electronics, Elements Mechanical Engineering, Basic concepts of Physics.

Course Learning Objectives: Students will be taught;

CLO1	Microsystems and applications.
CLO2	Working principles of MEMS devices.
CLO3	Microsystem design and fabrication.
CLO4	Scaling in Electrostatic Forces and Electromagnetic Force.
CLO5	Micro manufacturing techniques.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Overview of MEMS and Microsystems: MEMS and Microsystem, Typical	L2
MEMS and Microsystems Products, Evolution of Microfabrication,	
Microsystems and Microelectronics, Multidisciplinary Nature of	
Microsystems, Miniaturization. Applications of Micro systems in	
Automotive industry, Applications of Microsystems in other industries.	
(Text-1: 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7 & 1.8)	
Module-2	8 Hours
Working Principles of Microsystems: Introduction, Microsensors-	L3
Biomedical sensors & Biosensors, Chemical sensors, Optical sensors,	
Pressure sensor and Thermal sensors. Microactuation- Actuation using	
thermal force, shape memory alloys, piezoelectric crystals and electrostatic	
force. MEMS with Microactuators- Microgippers, Micromotors and	
Micropumps. Microaccelerometers, Microfluidics. (Text-1: 2.1, 2.2, 2.2.2,	
2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.3, 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.4, 2.4.1, 2.4.2, 2.4.4,	
2.5, 2.6)	
Module-3	8 Hours
Engineering Science for Microsystems Design and Fabrication:	L3
Introduction, Ions and Ionization, Molecular Theory of Matter and Inter-	
Molecular Forces, Plasma Physics, Electrochemistry-Electrolysis. (Text 1:	
3.1, 3.3, 3.4, 3.7, 3.8, 3.8.1)	
Engineering Mechanics for Microsystems Design: Introduction, Static	
Bending of Thin Plates, Overview on Finite Element Stress Analysis. (Text-1:	
4.1, 4.2 & 4.7)	_
Module-4	8 Hours
Scaling Laws in Miniaturization: Introduction, scaling in Geometry, scaling	L3
in Rigid-Body Dynamics-scaling in dynamic force, trimmer force scaling	
vector. Scaling in Electrostatic Forces, scaling in Electromagnetic Force,	
scaling in Electricity, scaling in Fluid Mechanics, scaling in Heat Transfer-	
scaling in heat conduction and scaling in heat convection.	
(Text-1: 6.1, 6.2, 6.3, 6.3.1, 6.3.2, 6.4, 6.5, 6.6, 6.7, 6.8 & 6.8.2)	



Module-5	8 Hours
Overview of Micromanufacturing: Introduction, Bulk Micromanufacturing-	L3
over view of Etching, Isotropic and Anisotropic etching, Wet etchants, Etch	
stop, Dry etching, Comparison of wet versus dry etching. Surface	
Micromachining- General description, Process in general, Mechanical	
problems associated with surface micro machining. The LIGA Process-	
General description of the LIGA process, Material for substrates and	
photoresists. Electroplating. SLIGA process. Summary of	
Micromanufacturing. (Text-1: 9.1, 9.2, 9.2.1, 9.2.2,9.2.3, 9.2.4, 9.2.5, 9.2.6,	
9.3.1, 9.3.2, 9.3.3, 9.4, 9.4.1, 9.4.2, 9.4.3, 9.4.4, 9.5, 9.5.1, 9.5.2 & 9.5.3)	

CO1	Explain Microsystems used in MEMS and their application areas.
CO2	Describe the working principles of MEMS devices.
CO3	Develop mathematical and analytical models of MEMS devices.
CO4	Discuss the scaling in fabrication of MEMS devices
CO5	Describe the different Micromanufacturing techniques used in Mems devices
	development.

Textbook:

1. Tai-Ran Hsu, MEMS and Micro systems: Design and Manufacture, 2nd Edition, 8th reprint, Tata Mc Graw-Hill Edition, 2002.

Reference Books:

- 1. Hans H. Gatzen, Volker Saile and JurgLeuthold, Micro and Nano Fabrication: Tools and
- 2. Processes, Springer, 2015.
- 3. Dilip Kumar Bhattacharya and Brajesh Kumar Kaushik, Microelectromechanical Systems, Cengage Learning India Private Limited, 2015

MOOCs:

- 1. https://www.nptelvideos.com/video.php?id=788
- 2. https://www.youtube.com/watch?v=j9y0gfN9WMg
- 3. https://www.youtube.com/watch?v=EALXTht-stg
- 4. https://www.youtube.com/watch?v=unj23A8br0U

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1



Table 1: Distribution of weightage for CIE & SEE of Regular courses.

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	-	-	1	1	1	-	-	ı			
CO2	3	2	1	-	-	1	1	1	-	-	-			
CO3	3	2	1	-	-	1	1	1	-	-	ı			
CO4	3	2	1	-	-	1	1	1	-	-	-			
CO5	3	2	1	-	-	1	1	1	-	-	-			
Average	3	2	1	-	-	1	1	1	-	-	-			



SEMESTER – VI Program Electives-2

Course: Microwave and Radar

Course Code	22ECE644	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught.

	<u> </u>
CLO1	High frequency microwave lines.
CLO2	Microwave diodes and operation.
CLO3	Microwave networks and passive devices.
CLO4	Radar fundamentals and analyze the radar signals.
CLO5	Various technologies involved in the design of radar transmitters and receivers.

Content	No. of
	Hours/RBT
	levels
Module 1	8 Hours
Microwave transmission lines: Introduction, transmission lines equations and	L2
solutions, reflection and transmission coefficients, standing waves and SWR, line	
impedance and line admittance. Smith chart, impedance matching using single stubs,	
Microwave coaxial connectors. (Text-1: 3.1-3.5 & 3.7)	
Module 2	8 Hours
Microwave diodes: Transfer electron devices: Introduction, GUNN effect diodes –	L3
GaAs diode, RWH theory, Modes of operation, Avalanche transit time devices: READ	
diode, IMPATT diode, BARITT diode, Parametric amplifiers Other diodes: PIN diodes,	
Schottky barrier diodes(Text-1: 10.1-10.8)	
Module 3	8 Hours
Microwave network theory: Microwave network theory and passive devices.	L3
Symmetrical Z and Y parameters, for reciprocal Networks, S matrix representation of	
multi-port networks.	
Microwave passive devices: Microwave passive devices, Coaxial connectors and	
adapters, Phase shifters, Attenuators, Waveguide Tees, Magic tees. (Text-1: 6.1-6.4)	
Module 4	8 Hours
Basics of Radar: Introduction, Maximum Unambiguous Range, Simple form of Radar	L3
Equation, Radar Block Diagram and Operation, Radar Frequencies and Applications,	
Prediction of Range Performance, Minimum Detectable Signal, Receiver Noise,	
Modified Radar Range Equation, Illustrative Problems. Radar Equation: SNR,	
Envelope Detector, False Alarm Time and Probability, Integration of Radar Pulses,	
Radar Cross Section of Targets (simple targets – sphere, cone-sphere (Text-2: 1.1-1.4,	
1.6, 2.1-2.3 & 2.5-2.7)	

Module 5						
CW and Frequency Modulated Radar: Doppler Effect, CW Radar – Block Diagram,						
Isolation between Transmitter and Receiver, Non-zero IF Receiver, Receiver						
Bandwidth Requirements, Applications of CW radar, Illustrative Problems.FM-						
CW Radar, Range and Doppler Measurement, Block Diagram and Characteristics						
(Approaching/ Receding Targets), FM-CW altimeter, Multiple Frequency CW Radar.						
(Text-2: 3.1-3.3 & 3.5)						

CO1	Understand the working principles of high frequency transmission lines.
CO2	Discuss the working principles of microwave diodes.
CO3	Explain the microwave passive devices and network theory.
CO4	Discuss the radar fundamentals and radar signals.
CO5	Explain the working principle of pulse Doppler radars, their applications and limitations.

Textbooks:

- 1. Annapurna Das, Sisir K Das, Microwave Engineering, 2nd Edition, TMH Edition, 2009.
- 2. Merrill I. Skolnik, Introduction to Radar Systems, 2nd Edition, TMH Special Indian Edition, 2007.

Reference Books:

- 1. Byron Edde, Radar Principals Technology Applications, 3rd Edition, Pearson Education, 2004.
- 2. Peebles, Jr., Radar Principles, 3rd Edition, P.Z.Wiley, 1998.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total			
			Marks			
	CIE Test-1	40				
CIE	CIE Test-2	40	F0			
CIE	CIE Test-3	40	50			
	Assignments	10				
SEE	Semester End Examination	50	50			
	Grand Total					

	CO-PO and PSO Mapping													
CO/PO	PO1	P02	PO3	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PSO1	PS02
CO1	1	2	-	2	-	-	-	-	-	-	1	1	2	-
CO2	2	2	-	2	-	-	-	-	-	-	1	1	2	-
CO3	2	2	-	2	-	-	-	-	-	-	1	1	2	-
CO4	2	2	-	2	-	-	-	1	-	-	1	1	2	1
CO5	2	2	-	2	-	-	1	1	-	-	1	1	2	-
Average	2	2	-	2	-	-	-	1	_	-	1	1	2	-



SEMESTER – VI (Open Electives-other than ECE students)

Course: Communication Engineering

Course Code	21ECE651	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives Students will be taught;

CLO1	Essential elements of an electronic communications.
CLO2	Amplitude, Frequency & Phase modulations and Amplitude demodulation.
CLO3	Basics of sampling and quantization.
CLO4	Various digital modulation schemes and Source and Channel Coding techniques.
CLO5	Principles of wireless communications system.

Content	No. of Hours / RBT Level
Module -1	8 Hours
Introduction to Electronic Communications: Historical perspective,	L2
Electromagnetic frequency spectrum, signal and its representation,	
Elements of electronic communications system, primary communication	
resources, signal transmission concepts, Analog and digital transmission,	
Modulation, Concept of frequency translation, Signal radiation and	
propagation. (Text 1: 1.1 to1.10)	
Module -2	8 Hours
Noise: Classification and source of noise (Text1:3.1)	L2
Amplitude Modulation Techniques: Types of analog modulation, Principle	
of amplitude modulation, AM power distribution, Limitations of AM	
Analog Transmission and Reception: AM Radio transmitters, AM Radio	
Receivers. (Text 1: 3.1, 4.1, 4.2, 4.4, 4.6, 6.1 & 6.2)	
Module -3	8 Hours
Sampling Theorem and pulse Modulation Techniques: Digital Versus	L2
Analog Transmissions, Sampling Theorem, Classification of pulse	
modulation techniques, PAM, PWM, PPM, PCM. (Text 1: 7.2 to 7.6)	
Module -4	8 Hours
Digital Modulation Techniques: Types of digital Modulation, ASK, FSK, PSK, QPSK.	L2
Source and Channel Coding: Objective of source coding, source coding	
technique, Shannon's source coding theorem, need of channel coding,	
Channel coding theorem, error control and coding. ((Text 1: 9.1 to 9.5, 11.1	
to 11.3, 11.8, 11.9 &11.12)	
Module -5	8 Hours
Evolution of wireless communication systems: Brief History of wireless	L2
communications, Advantages of wireless communication, disadvantages	
of wireless communications, wireless network generations, Comparison of	

wireless systems, Evolution of next generation networks, Applications of wireless communication.

Principles of Cellular Communications: Cellular terminology, Cell structure

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells and Frequency reuse distance. (Text 2: 1.1 to 1.7, 4.1 to 4.7)

Course Outcomes: Upon completion of this course, student will be able to:

CO1	Describe operation of communication systems.
CO2	Explain the techniques of Amplitude and Angle modulation.
CO3	Describe the concept of sampling and quantization.
CO4	Explain the concepts of different digital modulation techniques.
CO5	Describe the principles of wireless communications system.

Text books:

1. T L Singal, Analog and Digital Communications McGraw Hill Education (India) Private Limited, 1st Edition, 2012.

Reference Books:

- 1. B. P. Lathi, Modern Digital and Analog Communication Systems Oxford University Press, 4th Edition, 2010.
- 2. R.P. Singh and S. Sapre, Communication Systems: Analog and Digital, TMH, 2nd edition, 2007.
- 3. Gray J Mullett, Introduction to Wireless Telecommunications systems and Networks Cengage learning, 1st Edition, 2006.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	Ε0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		



	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	-	-	-	ı	ı	-	-	-		2	1
CO2	3	2	1	-	1	1	1	1	ı	-	-		2	1
CO3	3	2	1	-	1	1	1	1	ı	-	-		2	1
CO4	3	2	1	-	-	-	-	-	-	-	-		2	1
CO5	3	2	1	-	1	-	ı	1	-	-	-		2	1
Average	3	2	1	-	-	-			-	_	-		1	1

Low-1: Medium-2: High-3



SEMESTER –VI (Open Electives-other than ECE students)

Course: Electronic Circuits with Verilog

Course Code	22ECE652	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	To impart the concepts of simplifying Boolean expression using K-map techniques.
CLO2	To impart the concepts of designing and analyzing combinational logic circuits.
CLO3	To impart design methods and analysis of sequential logic circuits.
CLO4	To impart the concepts of Verilog HDL-data flow models for the design of digital
	systems.
CLO5	To impart the concepts of Verilog HDL- models using behavioral and structural
	description.

Content	No. of Hours / RBT levels
Module 1	08 Hours
Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL flow, why Verilog HDL?, trends in HDLs. (Text 1)	L2
Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. (Text 1)	
Module 2	08 Hours
Basic Concepts: Lexical conventions, datatypes, system tasks, compiler directives. (Text 1) Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing. (Text 1)	L2
Module 3	08 Hours
Gate-Level Modeling: Modeling using basic Verilog gate primitives,	L3
description of and/or and buf/not type gates, rise, fall and turn-off delays,	
min, max, and typical delays. (Text1)	
Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types. (Text 1)	
Module 4	08 Hours
Behavioral Description: Behavioral Description Highlights, Structure of	L3
the HDL Behavioral Description, Sequential Statements, IF Statement, The	
case Statement , Verilog casex and casez The wait-for Statement. The Loop	
Statement, For-Loop, While-Loop, Verilog repeat, Verilog forever (content	
with respect to Verilog only) (Text 2)	
Module 5	08 Hours
Structural Description: Highlights of Structural Description, Organization	L3
of Structural Description Binding (4.1, 4.2, 4.3 till example 4.9) (Text 2)	
Tasks and Functions: Differences between tasks and functions,	
declaration, invocation, automatic tasks and functions. (Text 1)	



CO1	Understand the Verilog HDL design flow.
CO2	Describe the basic concepts of Verilog HDL programming.
CO3	Design of digital electronics circuits using dataflow, behavioural, gate-level, and
	structural modelling.
CO4	Design complex digital circuits using advanced Verilog concepts.
CO5	Develop Verilog description using structural description for digital circuits.

Textbooks:

- 1. "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.
- 2. "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	Ε0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	Grand Total		100

	CO-PO and PSO Mapping													
COs	P01	P02	PO3	P04	P05	P06	P07	P08	P09	PO10	P011	PO12	PS01	PS02
CO1	3	2	1	-	-	1	1	1	-	-	-			
CO2	3	2	1	ı	ı	1	1	1	-	-	-			
CO3	3	2	1	ı	1	1	1	1	-	-	-			
CO4	3	2	1	-	-	1	1	1	-	-	-			
CO5	3	2	1	-	-	1	1	1	_	-	-			
Average	3	2	1	-	-	1	1	1	_	_	-			



SEMESTER –VI (Open Electives-other than ECE students)

Course: Microcontroller and its Applications

Subject Code	22ECE653	CIE Marks	50
Hours/Week (L: T: P)	3:0:2	SEE Marks	50
No. of Credits	4	Examination Hours	03

CLO1	The architecture, addressing modes and memory interfacing of 8051 microcontroller.
CLO2	Instruction set and programming of 8051 microcontroller.
CLO3	The operation of 8051 Timers/Counters, serial port and programming.
CLO4	The operation of 8051 interrupts and its programming.
CLO5	The 8255 PPI and the interfacing concepts.

Course Learning Objectives: Students will be taught;

Content	No. of Hours/ RBT levels
Module 1	8 Hours
8051 Microcontroller: Microprocessor Vs Microcontroller, Embedded	L2
Systems, 8051 Architecture-Registers, Pin diagram, I/O ports functions,	
Internal Memory organization. External Memory (ROM & RAM) interfacing,	
addressing Modes. (Text 1:1.1,3.1,3.2,3.3,5.1)	
Module 2	8 Hours
8051 Instruction Set and assembly programming: Data Transfer	L3
instructions, Arithmetic instructions, Logical instructions, Branch	
instructions, Bit manipulation instructions. Jump and call instructions,	
subroutines, and Assembly level language Program examples. (Text	
1:5.2,5.3,5.4,5.5,chapter 6 full,7.3,7.4,7.5,7.6,8.1,8.2,8.3)	
Module 3	8 Hours
8051 Timer and Serial Port Programming in assembly and C: Basics of	L3
Timers/Counters, Programming 8051 timers in assembly and C.	
Basics of serial communication, 8051 connection to RS 232, 8051 serial port	
programming in assembly and C. (Text 2:9.1,9.2,9.3,10.1,10.2,10.3,10.5)	_
Module 4	8 Hours
8051 Interrupts: 8051 Interrupts, Programming Timer Interrupts,	L3
programming external hardware interrupts, programming the serial	
communication interrupt, interrupt priority in the 8051. (All programs only	
in assembly) (Text 2:11.1,11.2,11.3,11.4,11.5)	
Module 5	8 Hours
8255 PPI and Interfacing Applications: Block diagram and modes of	L3
8255 programmable peripheral Interface. LCD interfacing, , ADC0808/0809,	ļ
DAC Interfacing, Stepper Motor Interfacing, DC Motor (All programs are	
only in C). (Text 2:12.1,13.1,13.2,15.1,15.2,17.2,17.3)	

CO1	Explain the architecture, addressing modes and memory accessing of 8051
	microcontroller.
CO2	Explain the 8051 instruction set and Assembly level programs.
CO3	Develop the programming of 8051 Timers/Counters, serial communication in
	assembly / C programming.
CO4	Develop the 8051 interrupt programming in assembly.
CO5	Write programs for interfacing applications.

Text Books:

- 1. Kenneth J. Ayala, The 8051 Microcontroller, 3rd Edition, Thomson/Cengage Learning.
- 2. Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay, The 8051 Microcontroller and Embedded Systems using assembly and C, 2nd Edition, Pearson Education, 2006.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Table 2: 2 to the date of the							
	Component	Marks	Total					
			Marks					
	CIE Test-1	40						
CIE	CIE Test-2	40	F0					
CIE	CIE Test-3	40	50					
	Assignments	10						
SEE	Semester End Examination	50	50					
	Grand Total		100					

	CO-PO and PSO Mapping													
COs	P01	P02	P03	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PS01	PS02
CO1	2	-	2	-	-	-	-	-	-	-	-	-	-	-
CO2	2	2	-	-	-	-	-	-	-	-	-	1	-	-
CO3	2	1	2	-	-	-	-	-	-	-	-	1	-	-
CO4	2	1	-	-	-	-	-	-	-	-	-	1	-	1
CO5	2	1	2	-	-	-	-	-	-	-	-	1	-	-
Average	2	1	2									1	-	-



SEMESTER –VI (Open Electives-other than ECE students)

Course: Internet of Things

Course Code	22ECE654	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Objectives: Students will be taught;

CLO1	Main components of IoT
CLO2	Enabling technologies
CLO3	IoT Processing Topologies and Connectivity technologies
CLO4	IoT Communication technologies
CLO5	IoT case studies and Future trends.

Content	No. of Hours/ RBT levels
Module 1	
Introduction to IoT: Introduction and definition of IoT; -Basics of networking:	8 Hours
Network types; Layered network models; Addressing; TCP/IP Transport layer;	L2
Predecessors of IoT: WSN; M2M; Cyber Physical Systems (Text 1: chapter 1, 3)	
IoT Enabling Technologies: Sensors, Cloud computing; Big data analytics;	
Embedded systems; IoT levels: level 1 to level 6 (Text 2: chapter 1)	
Module 2	8 Hours
Introduction to Sensors; actuators; microcontrollers, and their interfacing:	L3
Sensors-characteristics, types; Sensor interfacing-interfacing gas sensors, pH	
sensor, ultrasonic sensor with NodeMCU/ Arduino. Actuators: types, functions;	
Microcontrollers and overview. (Text 1: chapter 5, Text 2:chapter 2)	
Module 3	
IoT Processing Topologies and Types: Data format, Importance of Processing	8 Hours
in IoT, Processing Topologies, IoT device design and selection considerations,	L3
Processing Offloading (Text 1: chapter 6)	
IoT connectivity Technologies: IEEE 802.15.4; Zigbee; RFID; NFC; Sigfox; LoRa;	
NB-IoT; WiFi; Bluetooth (Text 1: chapter 7)	
Module 4	8 Hours
IoT Communication Technologies: -Constrained nodes and networks: types;	L3
lossy and low power networks (Text 1: chapter 8)	
Protocols for messaging and transport : Messaging protocols- MQTT; CoAP;	
XMPP; DDS -Protocols for addressing and identification: IPV4; IPV6; Uniform	
Resource Identifier (URI) (Text 2:chapter 3,4)	
Module 5	8 Hours
IoT Case studies and Future trends: Agricultural IoT; Vehicular IoT;	L2
Healthcare IoT; Evolution of new IoT paradigms- IoBT; IoV; IoNT; IoD; IoSpace	
(Text 1: chapter 12,15)	



CO1	Explain the term IoT and understand the main components of IoT systems						
CO2	Apply various enabling technologies, connectivity technologies and communication						
	protocols that occur in IoT systems						
CO3	Design and analysis of a complete working IoT system involving prototyping,						
	programming and data analytics						
CO4	Analyze lossy & low power networks and protocols.						
Co4	Analysis of various case studies						

Text Books:

- 1. Shriram K Vasudevan; Abhishek S Nagarajan; RMD Sundaram, Internet of Things, 2nd Edition, Wiley, New Delhi, 2020.
- 2. S. Mishra, A. Mukherjee, A. Roy, Introduction to IoT, 1st Ed., Cambridge University, UK, 2021

References:

- 3. A. Bahga, V. Madisetti, Internet of Things: A Hands-on approach, 1 st Ed., Universities Press (India) Pvt. Ltd., Hyderabad, 2014.
- 4. 4. K. N. Raja Rao (editor), Internet of Things: Concepts and Applications, 1 st ed., Wiley India, 2021.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE and SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
	CIE Test-2	40	
CIE	CIE Test-3	40	50
	Quiz 1/AAT	05	
	Quiz 2/AAT	05	
SEE	Semester End Examination	50	50
	100		



	CO-PO and PSO Mapping													
COs	PO1	PO2	PO3				PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2				1	1	-	2	-		-	-
CO2	3	2	2				1	-	-	1			-	-
CO3	3	2	3				2	1	-	3			-	-
CO4	3	2	2				2	1						
CO5	3	3	3				2	1		2				
Average	3	2	2				2	1	-	2			ı	-

SEMESTER - V/VI

Course: Environmental Science

Subject Code	22CIV57/66	CIE Marks	50
Hours/Week (L: T: P)	1:0:0	SEE Marks	50
No. of Credits	1	Examination Hours	1 hour

Course Learning Objectives: Students will be taught;

CLO1	The fundamentals of environmental science.
CLO2	The types of natural resources
CLO3	The various global environmental concerns.
CLO4	The types of wastes generated and their handling at a basic level
CLO5	The area of environmental law and policies with a few important acts in the field

	No. of	
Content	Hours/	
	RBT Levels	
Module 1		
Environment:		
Definition, scope & importance		
• Components of Environment Ecosystem: Structure and function of various		
types of ecosystems		
Human Activities – Food, Shelter, and Economic & Social Security.		
• Population - Growth, variation among nations - population explosion and		
impact on environment		
Biodiversity: Types, Value, Hot spots, Threats and Conservation of biodiversity,		
Forest Wealth, and Deforestation.		
Module 2	04 Hours /	
Natural Resources: Forest, Water, Mineral, Food, Energy, Land Environmental		
Pollution - Definition - causes, effects and control measures of: (a) Air pollution		
(b) Water pollution (c) Soil pollution (d) Marine pollution (e) Noise pollution (f)		
Thermal pollution (g) Nuclear hazards.		
Module 3	04 Hours /	
Global Environmental Concerns (Concept, policies and case-studies): Ground		
water depletion/recharging, Climate Change; Acid Rain; Ozone Depletion; Radon		
and Fluoride problem in drinking water; Resettlement and rehabilitation of		
people, Environmental Toxicology.		
Module 4	04 Hours /	
Sources: Sources of Solid waste, Types of solid waste, Physical and Chemical		
composition of municipal solid waste. Solid Waste Management Rules in India,		
Sources and management of E – Waste, Biomedical Waste, Hazardous waste, and		
construction waste at individual and community level.		
Socio-economic aspect of waste management Environmental Toxicology.		

Module 5						
Latest Developments in Environmental Pollution Mitigation Tools (Concept and	L2					
Applications): Environment Impact Assessment, Environmental Management						
Systems, ISO14001; Environmental Stewardship, NGOs.						

C01	Understand holistically the key concepts "Environment", and "Biodiversity".
CO2	Classify the types of natural resources available and the effects of anthropogenic interventions.
C03	Express the gravity of various global environmental concerns.
CO4	Categorize the types of wastes generated and their handling at a basic level.
CO5	Understand the importance of environmental law and policies.

Textbooks:

- 4. Environmental studies, Benny Joseph, Tata Mcgraw-Hill 2nd edition 2012
- 5. Environmental studies, S M Prakash, pristine publishing house, Mangalore 3rd edition-2018
- 6. Gilbert M.Masters, Introduction to Environmental Engineering and Science, 2nd edition, Pearson Education, 2004

Reference books:

- 1. Benny Joseph, Environmental studies, Tata Mcgraw-Hill 2nd edition 2009
- 2. M.Ayi Reddy, Textbook of Environmental Science and Technology, BS publications
- 3. 2007 Dr. B.S Chauhan, Environmental Studies, University of science press 1st edition

Web References:

https://www.hzu.edu.in/bed/E%20V%20S.pdf

https://onlinecourses.nptel.ac.in/noc23_hs155/preview

https://onlinecourses.swayam2.ac.in/cec19_bt03/preview

Scheme of Examination:

Semester End Examination (SEE): SEE Question paper is to be set for 50 marks with multiple choice questions of 1 mark each covering all aspects of the syllabus.

Continuous Internal Evaluation (CIE): Three Tests are to be conducted for 50 marks each. The average of the three tests are taken for computation of CIE. Question paper for each of the CIE is to be of the multiple-choice type with 50 question each.

Typical Evaluation pattern for regular courses is shown in Table 1.



Table 1: Distribution of weightage for CIE & SEE for 1 credit course

	Component	Marks	Total Marks
	CIE Test-1		
CIE	CIE Test-2	50	50
	CIE Test-3	50	
SEE	Semester End Examination	50	50
	Grand Total	100	

	CO/PO Mapping														
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1	PO11	PO12	PSO1	PSO2	PSO3
										0					
CO1	2	-	-	-	-	-	3	-	-	-	-	-	1	-	-
CO2	2	1	-	-	-	-	3	-	-	-	-	1	1	-	1
CO3	2	-	2	-	-	2	3	1	-	-	-	1	1	-	1
CO4	2	2	-	-	-	2	3	-	-	-	-	-	-	-	1
CO5	2	-	-	-	-	2	3	-	-	-	-	-	-	1	1
Average	2	1.5	2	-	-	2	3	1	-	-	-	1	1	1	1

Low-1: Medium-2: High-3



SEMESTER - V/VI

Course: Universal Human Values

Subject Code	22UHV57/66	CIE Marks	5
			0
Hours/Week (L: T: P)	1:0:0	SEE Marks	5
			0
No. of Credits	1	Examination Hours	1 hour

Course Learning Objectives: Students will be taught;

CLO1	To create an awareness on Engineering Ethics and Human Values.
CLO2	To understand social responsibility of an engineer.
CLO3	To appreciate ethical dilemma while discharging duties in professional life.

Module 1 Introduction to Value Education Value Education, Definition, Concept and Need for Value Education. The Content and Process of Value Education. Basic Guidelines for Value Education. Happiness and Prosperity as parts of Value Education. Module 2 Harmony in the Human Being Human Being is more than just the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the activities in the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. Human Rights violation and Social Disparities.		Content	No. of Hours
Introduction to Value Education Value Education, Definition, Concept and Need for Value Education. The Content and Process of Value Education. Basic Guidelines for Value Education, Self-exploration as a means of Value Education. Happiness and Prosperity as parts of Value Education. Module 2 Harmony in the Human Being Human Being is more than just the Body. Harmony of the Self ('I') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.		Module 1	
 Value Education, Definition, Concept and Need for Value Education. The Content and Process of Value Education. Basic Guidelines for Value Education, Self-exploration as a means of Value Education. Happiness and Prosperity as parts of Value Education. Module 2 Harmony in the Human Being Human Being is more than just the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 	Intr	oduction to Value Education	
 Basic Guidelines for Value Education, Self-exploration as a means of Value Education. Happiness and Prosperity as parts of Value Education. Module 2 Module 2 Harmony in the Human Being Human Being is more than just the Body. Harmony of the Self ('I') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 	•	Value Education, Definition, Concept and Need for Value Education.	110415
Self-exploration as a means of Value Education. Happiness and Prosperity as parts of Value Education. Module 2 Harmony in the Human Being Human Being is more than just the Body. Harmony of the Self ('I') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.	•	The Content and Process of Value Education.	
 Happiness and Prosperity as parts of Value Education. Module 2 Harmony in the Human Being Human Being is more than just the Body. Harmony of the Self ('1') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 	•	Basic Guidelines for Value Education,	
Module 2 Harmony in the Human Being Human Being is more than just the Body. Harmony of the Self ('I') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.	•	Self-exploration as a means of Value Education.	
Harmony in the Human Being Human Being is more than just the Body. Harmony of the Self ('1') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.	•	Happiness and Prosperity as parts of Value Education.	
 Human Being is more than just the Body. Harmony of the Self ('1') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 		Module 2	05
 Human Being is more than just the Body. Harmony of the Self ('1') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3	Har	mony in the Human Being	Hours
 Harmony of the Self ('1') with the Body. Understanding Myself as Co-existence of the Self and the Body. Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 	•	Human Being is more than just the Body.	1100110
 Understanding Needs of the Self and the needs of the Body. Understanding the activities in the Self and the activities in the Body. Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 	•		
Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.	•	Understanding Myself as Co-existence of the Self and the Body.	
Module 3 Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.	•	Understanding Needs of the Self and the needs of the Body.	
Harmony in the Family and Society and Harmony in the Nature Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.	•	Understanding the activities in the Self and the activities in the Body.	
 Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 		Module 3	05
 Family as a basic unit of Human Interaction and Values in Relationships. The Basics for Respect and today's Crisis: Affection, Guidance, Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 	Har	mony in the Family and Society and Harmony in the Nature	Hours
Reverence, Glory, Gratitude and Love, Comprehensive Human Goal: The Five Dimensions of Human Endeavour. Harmony in Nature: The Four Orders in Nature. The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.	•	Family as a basic unit of Human Interaction and Values in Relationships.	
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 The Holistic Perception of Harmony in Existence. Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 		•	
Module 4 Social Ethics The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct.		,	
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 The Basics for Ethical Human Conduct, Defects in Ethical Human Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 	Soc		
 Conduct. Holistic Alternative and Universal Order. Universal Human Order and Ethical Conduct. 			nours
Holistic Alternative and Universal Order.Universal Human Order and Ethical Conduct.		· · · · · · · · · · · · · · · · · · ·	
Universal Human Order and Ethical Conduct.			

Module 5						
Professional Ethics						
 Value based Life and Profession., Professional Ethics and Right 						
Understanding.						
Competence in Professional Ethics.						
 Issues in Professional Ethics – The Current Scenario. 						
Vision for Holistic Technologies						
Production System and Management Models.						

CO1	Understand the significance of value inputs in a classroom and start applying them intheir life and profession
CO2	Distinguish between values and skills, happiness and accumulation of physical facilities, the Self and the Body, Intention and Competence of an individual, etc.
CO3	Understand the role of a human being in ensuring harmony in society and nature.
CO4	Distinguish between ethical and unethical practices and start working out the strategy toactualize a harmonious environment wherever they work.

Textbooks:

- 1. A.N Tripathy, Human Values, New Age International Publishers, 2003.
- 2. Bajpai. B. L, Indian Ethos and Modern Management, New Royal Book Co, Lucknow, 2004
- 3. Bertrand Russe II, Human Society in Ethics & Politics

Reference books:

- 1. Corliss Lamont, Philosophy of Humanism.
- 5. Gaur. R.R., Sangal. R, Bagari G.P, A Foundation Course in Value Education, Excel Books, 2009.
- 6. I.C. Sharma, Ethical Philosophy of India, Nagin & co, Julundhar
- 7. William Lilly- Introduction to Ethics -Allied Publisher

Scheme of Examination:

Semester End Examination (SEE): SEE Question paper is to be set for 50 marks with multiple choice questions of 1 mark each covering all aspects of the syllabus.

Continuous Internal Evaluation (CIE): Three Tests are to be conducted for 50 marks each. The average of the three tests are taken for computation of CIE. Question paper for each of the CIE is to be of the multiple-choice type with 50 question each. Typical Evaluation pattern for regular courses is shown in Table 1.

Table 1: Distribution of weightage for CIE & SEE for 1 credit course

	Component	Marks	Total Marks
	CIE Test-1	50	
CIE	CIE Test-2	50	50
	CIE Test-3	50	
SEE	Semester End Examination	50	50
	Grand Total	100	



	CO/PO Mapping															
CO/PO	PO1	PO2	PO3	P04	PO5	P06	P07	P08	P09	PO10	PO11	PO12	PS01	PS02	PSO3	PS04
CO1	-	-	1	-	-	1	-	2	ı	-	-	1	-	-	-	-
CO2	-	-	-	-	-	-	-	2	-	-	-	1	-	-	-	-
CO3	-	1	-	-	1	-	-	2	-	-	-	1	-	-	-	-
CO4	-	-	1	-	-	1	-	2	ı	-	-	1	-	-	-	-
Average	-	ı	ı	-	1		-	2	ı	ı	-	1	-	-	-	-

Low-1: Medium-2: High-3



SEMESTER - VI

Course: VLSI Laboratory

Subject Code	22ECEL67	CIE Marks	50
Hours/Week (L: T: P)	0:0:2	SEE Marks	50
Credits	1	Examination Hours	03

Course Learning Objectives: Student will be taught;

CLO1	Designing, modeling, simulating and verifying CMOS digital circuits.
CLO2	Designing layouts and performing physical verification of CMOS digital
	circuits.
CLO3	Analyzing ASIC design flow and understanding the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
CLO4	Performing RTL-GDSII flow and understanding the stages in ASIC design.

Sl. No	PART – A	RBT levels
	Analog Design (Back end)	
1. (a)	Capture the schematic of CMOS inverter with load capacitance of	L3
	0.1pF and set the widths of inverter (Wn/Wp) and length at selected	
	technology.	
	Observe the input and output voltage for the designed inverter. Also	
(b)	compute tpHL, tpLH and td.	
	Draw the layout of the inverter. Verify for DRC and LVS, extract	
	parasitic and perform post layout simulations, compare the results	
2 ()	with pre-layout simulations. Record the observations.	
2. (a)	Capture the schematic of 2-input CMOS NAND gate. Verify the	
	functionality of NAND gate and also find out the delay td for all four	L3
(1-)	possible combinations of input vectors. Table the results.	
(b)	Draw layout of NAND gate. Verify for DRC and LVS, extract parasitic	
	and perform post layout simulations, compare the results with pre-	
2 (2)	layout simulations. Record the observations.	L3
3.(a)	Capture the schematic of Common Source Amplifier. Find its Transient response, DC response and AC response. Calculate Gain	L3
(b)	and Bandwidth.	
(5)	Draw layout of common source amplifier. Verify for DRC and LVS,	
	extract parasitic and perform post layout simulations, compare the	
	results with pre-layout simulations. Record the observations.	
	Part – B	
	Digital Design (Front end)	
1.	Write Verilog code for 4-bit up/down asynchronous reset counter	L3
	and carry out the followings:	
	a. Verify the functionality using test bench	
	b. Synthesize the design by setting area and timing constraint.	
	Obtain the gate level netlist. Record the area requirement in terms	
	of number of cells required power and area requirement.	
2.	Write Verilog code for 4-bit adder and verify its functionality using	L3
	test bench. Synthesize the design by setting proper constraints and	

J.

	obtain the net list. From the report generated identify, total number	
	of cells, power requirement and total area required.	
3.	Write Verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (SR, JK, D, T).	L3
4.	For the synthesized netlist carry out the following for any one of the above experiments: a. Floor planning (automatic), identify the placement of pads b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells. c. Physical verification and record the LVS and DRC reports. d. Perform Back annotation and verify the functionality of the design. e. Generate GDSII and record the number of masks and its color composition.	L3

CO1	Demonstrate ASIC design flow and understand the process of synthesis, synthesis
	constraints and evaluating the synthesis reports to obtain optimum gate level net
	list.
CO2	Design and simulate basic CMOS circuits like inverter, NAND gate and common
	source amplifier.
CO3	Design and simulate combinational and sequential digital circuits using Verilog HDL.
CO4	Illustrate the Synthesis process of digital circuits using EDA tool.
CO5	Perform RTL-GDSII flow and understand the stages in ASIC design.

Textbooks:

- 1. Sung Mo Kang and Yosuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3rd Edition, Tata McGraw-Hill.
- 2. Neil H. E. Weste and David Money Harris CMOS VLSI Design- A Circuits and Systems Perspective, 4th Edition, Pearson Education, 2011.

Scheme of Examination:

Semester End Examination (SEE):

- 1. All laboratory experiments are to be included for practical examination.
- 2. Students can pick one experiment from the questions lot prepared by the examiners.
- 3. Change of experiment is allowed only once and 20% Marks allotted to the write up part to be made zero.

Semester End Examination Evaluation							
SL.NO	ACTIVITY	MARKS					
1	Write-Up	15					
2	Conduction	70					
3	Viva Voce	15					
	TOTAL	100					

Note: The marks scored will be proportionately reduced to 50

Continuous Internal Evaluation (CIE):

As part of CIE process, progressive continuous evaluation is done for laboratory work on weekly basis of conduct of experiment by student either individually or in group based on the laboratory. The breakup of the marks allocated is given in the Table-1.

	, ,				
Table-1 WEEKLY EVALUATION OF CONDUCT OF EXPERIMENT					
SL.NO	ACTIVITY	MAX MARKS			
1	Conduct of experiment and documentation	10			
2	Analysis & interpretation of results	5			
3	Viva voce	5			
•	TOTAL				

Internal exam conducted at the end of the semester or on completion of a predefined set of experiments based on the laboratory. The evaluation detail of laboratory internal exam is given in Table-2

	Table-2 LAB INTERNAL EXAM						
SL.NO	ACTIVITY	MAX MARKS					
1	Detailed write-up about the experiment with relevant procedure	5					
	and calculation.						
2	Conduction of experiment	20					
3	Viva voce	5					
	TOTAL						

	TABLE-3 FINAL CIE CALCULATION					
SL.NO	METRICS USED	MAX MARKS				
1	1 Average of all weekly evaluation of conduct of experiment					
2	2 LAB Internal Exam					
	TOTAL					

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	1	3				-	ı	1	2	3	3
CO2	3	2	2	1	3				3		ı	2	3	3
CO3	3	2	2	1	3				3		ı	2	3	3
CO4	3	2	2	1	3				3		ı	2	3	3
CO5	3	2	2	1	3				3		ı	2	3	3
Average	3	2	2	1	3				3		-	2	3	3

Low-1: Medium-2: High-3

SEMESTER - VI

Course: Mini Project

Subject Code	22ECEMP68	CIE Marks	50
Hours/Week (L: T: P)	0:0:2	SEE Marks	50
Credits	2	Examination Hours	03

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

- (i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide. The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
- (ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all the guides of the college. The CIE marks awarded for the Miniproject, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE for Mini-project:

- (i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester end examination (SEE) conducted at the department.
- (ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.



IV-YEAR ECE SYLLABUS-2022 SCHEME



Department of Electronics and Communication Engineering

GLOBAL ACADEMY OF TECHNOLOGY

(Autonomous institution affiliated to VTU, Belagavi.
Accredited by NAAC with 'A' grade,
NBA Accredited CS, E&C, E&E, MECH, CV and IS branches)
Ideal Homes Township,
Raja Rajeshwari Nagar, Bengaluru-560098.

Global Academy of Technology, Bengaluru

(Autonomous Institution Affiliated to VTU)

Scheme of Teaching and Examination 2022-23

Electronics and Communication Engineering

VII SEMESTER -UG

SI.	Course	Course Title	Course	Teaching	nouis/ week		Ex	aminat	CREDITS		
No.	Code	Code Type Dept.		Dept.	L	Т	P	CIE	SEE	Total	
1	22ECE71	Advanced VLSI	PC		3	0	0	50	50	100	3
2	22ECE72	Computer Communication Networks (Integrated)	IPC	Respective	3	0	2	50	50	100	4
3	22ECE73	Antenna and Wave propagation (Integrated)	IPC	Department	3	0	2	50	50	100	4
4	22ECE74X	Program Elective-3	PEC		3	0	0	50	50	100	3
5	22ECE75X	Open Elective-2	OEC	Offering Department	3	0	0	50	50	100	3
6	22ECEP76	Project Work Phase-I	MP	Two Contact hours per week			100	-	100	2	
	TOTAL 350 250 600							19			

Program Elective-3*									
22ECE741	Cryptography	22ECE743	Optical Fiber Communication						
22ECE742	Machine Learning with Python	22ECE744	Biomedical Signal Processing						
	Open Elective-2 (Offered to other branch students)								
22ECE751	Wireless and Mobile Networks	22ECE753	Basic VLSI Design						
22ECE752	Automotive Electronics	22ECE754	Smart Sensors & Instrumentation						

*NPTEL for Credit transfer: Students can take 12 weeks NPTEL course as an equivalent to Program elective. The NPTEL courses of duration less than 12 weeks will not be considered for credit transfer. The courses (only technical) taken are as per the recommendation of BOS of respective department. The similarity of the contents as offered by NPTEL should not exceed a maximum of 40% of the courses being registered by the student. The NPTEL course need to be completed before the registration of the elective. Any certificate obtained after the registration of elective would not be considered. The validity of NPTEL certificate is for two years and it cannot be used more than once to avail the benefit. The student is eligible to transfer a maximum of nine credits in the entire duration of the program. The grades will be awarded as equivalent to the grades obtained in the NPTEL course.



Global Academy of Technology, Bengaluru

(Autonomous Institution Affiliated to VTU)

Scheme of Teaching and Examination 2022-23 Electronics and Communication Engineering

VIII SEMESTER -UG											
SI.	Course	Course Title Course				Teaching Hours/Week			aminat	CREDITS	
No.	Code		Туре	Type Dept.		Т	Р	CIE	SEE	Total	
1	22ECE81	Cellular and Mobile Communication	PC	Respective	4	0	0	50	50	100	4
2	22ECE82X	Program Elective-4	PEC Department PEC		3	0	0	50	50	100	3
3	22ECE83X	Program Elective-5			3	0	0	50	50	100	3
4	22ECEP84	Project Work Phase –II	MP	Two Contact hours per week			100	100	200	8	
5	22ECES85	Technical Seminar	MP	One Contact hour per week			100		100	1	
6	22INT86	Internship	INT	Completed during the intervening period of VI and VII Semester			100		100	2	
	TOTAL 450 250 700 2								21		

Program Elective-4*									
22ECE821	Network and Cyber Security	22ECE823	ASIC Design						
22ECE822	DSP Algorithms and Architecture	22ECE824	Wireless Sensor Networks						
	Program Elective-5*								
22ECE831	Internet of Things and Cloud Computing	22ECE833	Multimedia Communication						
22ECE832	High Performance Computer Networks	22ECE834	Digital Switching systems						

*NPTEL for Credit transfer: Students can take 12 weeks NPTEL course as an equivalent to Program elective. The NPTEL courses of duration less than 12 weeks will not be considered for credit transfer. The courses (only technical) taken are as per the recommendation of BOS of respective department. The similarity of the contents as offered by NPTEL should not exceed a maximum of 40% of the courses being registered by the student. The NPTEL course need to be completed before the registration of the elective. Any certificate obtained after the registration of elective would not be considered. The validity of NPTEL certificate is for two years and it cannot be used more than once to avail the benefit. The student is eligible to transfer a maximum of nine credits in the entire duration of the program. The grades will be awarded as equivalent to the grades obtained in the NPTEL course.



SEMESTER -VII

Course: Advanced VLSI

Course Code	22ECE71	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Analog Electronic Circuits, Design and Analysis of Digital Circuit and VLSI Design **Course Learning Objectives:** Students will be taught;

	0 ,
CLO1	Delay power calculations for VLSI circuits.
CLO2	Combinational circuit design
CLO3	Sequential circuit design and advanced techniques used in CMOS logic circuits.
CLO4	Various arithmetic circuits in CMOS VLSI design.
CLO5	System level physical design and testing of VLSI circuits.

Content	No. of Hours/ RBT levels
Module-1	8 Hours
Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths (Text 1: Chapter 4:4.1 to 4.5, except subsections 4.3.7, 4.4.5, 4.4.6, 4.5.4, 4.5.5 and 4.5.6). Power: Introduction, Low power architectures. (Text 1: Chapter 5: 5.1, 5.5)	L2, L3
Module-2	8 Hours
Combinational Circuit Design: Introduction, Circuit families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Pass-Transistor Circuits, Circuit pitfalls, threshold drops, ratio failures, leakage, charge sharing, power supply noise, hot spots, minority carrier injection. (Text 1: Chapter 9: 9.1, 9.2, 9.2.1, 9.2.2, 9.2.3, 9.2.5, 9.3.1 to 9.3.7)	L2, L3
Module-3	8 Hours
Sequential Circuit Design: Introduction, sequencing methods, Circuit Design for Latches and Flip Flops. (Text 1: Chapter 10:10.1, 10.2.1, 10.3.1 to 10.3.5) Advanced Techniques in CMOS Logic Circuits: Mirror Circuits, PseudonMOS, Tri-state circuits, Dynamic CMOS logic circuits. (Text 2: Chapter 9: 9.1, 9.2, 9.3 & 9.5)	L2, L3
Module-4	8 Hours
Arithmetic Circuits in CMOS VLSI: Bit adder circuits, Ripple-Carry Adders, Other high speed adders, Carry skip circuits, carry select adders, Multipliers, array multipliers. (Text 2: Chapter 12: 12.1, 12.2, 12.4, 12.4.1, 12.4.2, 12.4.3, 12.5, 12.5.1)	L2, L3
Module-5	8 Hours
System level physical design: Large scale physical design, Floor planning and routing. (Text 2: Chapter 14: 14.1, 14.5) Reliability and Testing of VLSI Circuits: CMOS Testing, Test generation methods. (Text 2: Chapter 16: 16.2 & 16.3)	L2, L3

CO1	Understand delay power calculations in VLSI circuits.
CO2	Analyze combinational circuits.
CO3	Analyze Sequential circuit design and advanced techniques used in CMOS logic
	circuits.
CO4	Explore various arithmetic circuits in CMOS VLSI design.
CO5	Realize system level physical design and testing of VLSI circuits.

Textbooks:

- 1. Neil H. E. Weste, David Harris and Ayan Banerjee, CMOS VLSI Design- A Circuits and Systems Perspective, 4th Edition, Pearson Education 2011.
- 2. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & Sons.

Reference Books:

- 1. Adel Sedra and K. C. Smith, Microelectronics Circuits Theory and Applications, 7th Edition, Oxford University Press, International Version, 2009.
- 2. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Education (India) Private Limited, 2007.
- **3.** Sung Mo Kang and Yosuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3rd Edition, McGraw Hill Education (India) Private Limited.
- 4. Douglas A Pucknell and Kamran Eshaghian, Basic VLSI Design, 3rd Edition, Eastern Economy Edition 2006.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1.

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	0		
	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50



	CO-PO and PSO Mapping													
CO/PO	P01	P02	P03	P04	P05	P06	P07	P08	P09	PO10	P011	P012	PS01	PS02
CO1	3	3	3	-	1	-	1	-	-	-	-	2	2	2
CO2	3	3	3	-	1	-	-	-	-	-	2	2	2	2
CO3	3	3	3	-	1	-	-	-	-	-	2	2	2	2
CO4	3	3	3	-	1	-	-	-	-	-	2	2	2	2
CO5	3	3	3	-	1	-	1	-	-	-	2	2	2	2
Average	3	3	3	-	1	-	1	-	-	-	2	2	2	2

Low-1: Medium-2: High-3



SEMESTER - VII

Course: Computer Communication Networks (Integrated)

Course Code	22ECE72	CIE Marks	50
Hours/Week (L: T: P)	3:0:2	SEE Marks	50
No. of Credits	4	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	layering architecture of OSI reference model and TCP/IP protocol suite.
CLO2	Protocols associated with each layer.
CLO3	Different networking architectures and their representations.
CLO4	Functions and services associated with each layer.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Data Communications: Components, Representations, Data Flow, Networks: Physical Structures, Network Types: LAN, WAN, Switching and Internet. Network Models: Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP.	L3
(Text1:1.1, 1.2, 1.3, 2.1, 2.2 & 2.3.1)	
Module-2	8 Hours
Data-Link Layer: Introduction: Nodes and Links, Services, Categories of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking. Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. Controlled Access: Reservation, Polling, Token Passing, Channelization: FDMA, TDMA & CDMA (Text 1: 9.1, 9.2-9.2.1, 9.2.2, 11.1-11.1.1, 11.1.2, 11.2, 12.1, 12.2 & 12.3)	L3
Module-3	8 Hours
Wired LANs: Ethernet: Ethernet Protocol: IEEE802, Ethernet Evolution, Standard Ethernet: Characteristics, Addressing, Access Method, Efficiency, Implementation, Fast Ethernet: Access Method, Physical Layer, Gigabit Ethernet: MAC Sublayer, Physical Layer, 10 Gigabit Ethernet. Wireless LANs: Introduction: Architectural Comparison, Characteristics, IEEE 802.11: Architecture, MAC Sublayer, Addressing Mechanism, Physical Layer, Bluetooth: Architecture, Layers. (Text 1: 13.1, 13.2-13.2.1 to 13.2.5, 13.3, 13.4, 13.5, 15.1, 15.2 & 15.3)	L3
Module-4	8 Hours
Network Layer: Introduction, Network Layer services, Packet Switching, Datagram IPV4 Addresses, Forwarding of IP Packets Based on destination Address and Label. Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams, ICMPv4: Messages,	L3

Debugging Tools, Mobile IP: Addressing, Agents, Three Phases,	
Inefficiency in Mobile IP. Routing Algorithms: Distance Vector Routing,	<u> </u>
Link State Routing, Path vector routing.	l
Next Gen IP: IPV6 Addressing, ICMPv6. (Text 1:18.1, 18.2, 18.4, 18.5-	l
18.5.1, 18.5.2, 19.1.1 to 19.1.3, 19.2.1 to 19.2.2, 19.3, 20.2, 22.1 & 22.2)	l
Module-5	8 Hours
Transport Layer: Introduction: Transport Layer Services, Connectionless	L3
and Connection Oriented Protocols, Transport Layer Protocols: Simple	l
protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat	l
protocol.	l
User Datagram Protocol: User Datagram, UDP Services, UDP Applications.	l
Transmission Control Protocol: TCP Services, TCP Features, Segment,	l
Connection, State Transition diagram, Windows in TCP, Flow control, Error	<u> </u>
control, TCP congestion control, TCP Timers. (Text 1: 23.1, 23.2.1 to 23.2.4,	l
24 2 24 3 1 to 24 3 10)	Ì

	Practical Component of IPC							
PAR	RT-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/QualNet/							
F	Packet Tracer or any other equivalent tool.							
1.	Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.							
2.	Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.							
3.	Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data-rate.							
4.	Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.							
5.	Implementation of Link state routing algorithm.							
	PART-B: Implement the following in C/C++							
6.	Write a program for a HLDC frame to perform Bit stuffing and Character stuffing.							
7.	Write a program for distance vector algorithm to find suitable path for transmission.							
8.	Implement Dijkstra's algorithm to compute the shortest routing path.							
9.	Implementation of Stop and Wait Protocol and Sliding Window Protocol.							
10.	Write a program for congestion control using leaky bucket algorithm.							

CO1	Explain the concepts of networking.
CO2	Describe the various networking architectures.
CO3	Explain the protocols and services of different layers.
CO4	Describe the basic network configurations and standards associated with each
	network.
CO5	Analyze a simple network and measure its parameters.



Textbook:

1. Behrouz A Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013.

Reference Books:

- 1. James J Kurose and Keith W Ross, "Computer Networks", 7th Edition, Pearson Education, 2014.
- 2. Wayne Tomasi, "Introduction to Data Communication and Networking", 1st Edition. Pearson Education, 2015.
- 3. Andrew S Tanenbaum, "Computer Networks", 5th Edition, Prentice Hall, 2017.
- 4. William Stallings, "Data and Computer Communications", 8th Edition, Prentice Hall, 2017.

Scheme of Evaluation: (Integrated courses)

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of four sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question from each module.**

The laboratory assessment would be restricted to only the CIE evaluation.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. The average of the three tests are taken for computation of CIE on a scale of 30, the CIE would also include laboratory evaluation for 20 marks. The laboratory marks of 20 would comprise of 10 marks for regular laboratory assessment to include lab record and observation. 10 marks would be exclusive for laboratory internal assessment test to be conducted at the end of the semester. Typical Evaluation pattern for integrated courses is shown in Table-1.

	Component	Marks	Total Marks				
	CIE Test-1	30					
CIE	CIE Test-2	30	F0				
CIE	CIE Test-3	30	50				
	Laboratory	20					
SEE	Semester End	100	50				
	Examination						
	Grand Total						

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	ı	-	-	-	-	-	1		1	-	
CO2	3	2	-	-	-	-	-	-	-	1	-	1	-	-
CO3	3	2	-	-	-	-	-	-	-	1	1	1	-	ı
CO4	3	2	-	ı	-	-	-	-	-	1	ı	1	-	ı
CO5	3	2	-	-	-	-	-	-	-	1	-	1	-	-
Average	3	2	_	-	_	_	_	_	_	1	-	1	-	-

Low-1: Medium-2: High-3

SEMESTER -VII

Course: Antennas and Wave Propagation(Integrated)

Course Code	22ECE73	CIE Marks	50
Hours/Week (L: T: P)	3:0:2	SEE Marks	50
No. of Credits	4	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Basics of antenna theory.
CLO2	Field pattern of different types of antenna arrays.
CLO3	Short dipole and thin linear antenna.
CLO4	Types of antennas.
CLO5	Radio wave propagation.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Antenna Basics: Introduction, Basic antenna parameters, patterns, beam	L2
area, radiation intensity, beam efficiency, diversity and gain, directivity	
and resolution, antenna apertures, effective height, The radio	
communication link, fields from oscillating dipole, antenna field zones,	
antenna temperature, antenna impedance, front to back ratio, point	
sources, power patterns, power theorem. (Text-1: 2.1-2.13 & 4.1 to 4.4)	
Module-2	8 Hours
Point Sources and Arrays: Radiation intensity, Examples of power	L3
patterns, field patterns, phase patterns, Array of two isotropic point	
sources, pattern multiplication, nonisotropic and dissimilar point sources,	
Linear array of n isotropic point sources of equal amplitude and spacing,	
null directions for arrays of n isotropic point sources. (Text-1: 4.5 to 4.10 &	
4.12 to 4.14)	
Module-3	8 Hours
Electric Dipoles and Thin Linear Antenna: Introduction, short electric	L3
dipole, fields of a short dipole (no derivation of field components),	
radiation resistance of short dipole, thin linear antenna, and radiation	
resistances of lambda/2 Antenna. (Text-1: 5.1-5.6)	0.11
Module-4	8 Hours
Antenna Types: Introduction, small loop, comparison of far fields of small	L3
loop and short dipole, loop antenna general case, radiation resistance,	
patch antennas, Helical Antenna, helical geometry, horn antennas,	
rectangular horn antennas, Yagi-Uda array, parabolic reflectors, log	
periodic antenna, lens antenna. (Tex- 1: 6.1-6.4, 6.7, 6.18, 7.3, 7.4, 6.19,	
6.20, 7.7, 8.7, 9.7 &14.1)	
Module-5	8 Hours
Radio Wave Propagation: Radio wave propagation: Introduction, Ground	L2
wave propagation, free space propagation, ground reflection, surface	
wave, diffraction. Troposphere propagation, Tropospheric scatter,	
Ionospheric propagation, electrical properties of the ionosphere, effects	
of earth's magnetic field. (Text-2: 8.1.1-8.1.4, 8.1.6, 8.1.7, 8.2.1 & 8.2.2)	

	Practical Component of IPC							
	List of Experiments							
1	Conduct an experiment to measure the frequency and guide wavelength of microwave							
	test bench.							
2	Conduct an experiment to measure the power and attenuation in microwave test							
	bench.							
2	Conduct an experiment for the determination of VSWR of a horn antenna.							
3	Conduct an experiment to obtain the radiation pattern and measurement of directivity							
	& gain of microstrip dipole antenna.							
4	Conduct an experiment to obtain the radiation pattern and measurement of directivity							
	& gain of Yagi antennas.							
5	Conduct an experiment to obtain the radiation pattern and measurement of directivity							
	& gain of patch antenna.							
6	Conduct an experiment to determine:							
	a. Coupling and isolation characteristics of microstrip directional coupler.							
	b. Resonance characteristics of microstrip ring resonator and computation of dielectric							
	Constant of the Substrate.							
	c. Power division and isolation of microstrip power divider.							
7	Conduct an experiment to study V-I Characteristics of Gunn Diode.							
8	Conduct an experiment to study the Characteristics of Reflex Klystron.							
9	Conduct an experiment to analyse parameters of antenna using spectrum analyser.							

	Catedines. Open completion of this course, student will be usic to:
CO1	Describe antennas, their principle of operation, radiation pattern and applications.
CO2	Analyze antenna arrays and determine radiation patterns of different types of arrays.
CO3	Compare the radiation pattern of electric dipoles and thin linear antennas.
CO4	Select various antenna configurations according to the applications.
CO5	Identify different forms of radio wave propagation.

Textbooks:

- 1. John D. Krauss, Ronald J Marhefka and Ahmad S Khan, Antennas and Wave Propagation, 4th Special Indian Edition, McGraw- Hill Education Pvt. Ltd., 2010.
- 2. Harish and Sachidananda, Antennas and Wave Propagation, 3rd Edition, Oxford University Press, 2007.

Reference Books:

- 1. C.A. Balanis, Antenna Theory, 3rd Edition, John Wiley & Sons, 2005.
- 2. K.D. Prasad, Satya Prakashan, Antennas and Wave Propagation, 5th Edition, Tech India Publications, New Delhi, 2001.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment

Tools (AATs), and three tests. **Some possible AATs**: Seminar/assignments/ mini projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1.

Table 1: Distribution of weightage for CIE & SEE of Regular courses.

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50

	CO-PO and PSO Mapping													
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	1	-	-	-	-	-	-
CO2	3	2	-	-	-	1	-	1	-	-	-	-	2	-
CO3	3	1	-	-	-	1	-	1	-	-	-	-	-	-
CO4	3	2	-	1	-	1	-	1	-	-	-	1	2	ı
CO5	3	1	-	ı	-	1	_	-	-	-	-	1	2	-
Average	3	2	-	-	-	-	-	1	_	-	-	1	2	-

Low-1: Medium-2: High-3



SEMESTER –VII Program Elective-3

Course: Cryptography

Course Code	22ECE741	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites:

Course Objectives: Students will be taught;

CLO1	The classical encryption techniques and concepts of number theory.
CLO2	The various symmetric cipher techniques.
CLO3	The various asymmetric cipher techniques.
CLO4	Pseudo random sequence generators and One-Way hash functions.
CLO5	Message authentication codes and Digital signatures.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Classical Encryption Techniques: Symmetric cipher model, Substitution	L2, L3
techniques, Transposition techniques.	ļ
Basic Concepts of Number Theory and Finite Fields: Euclidean algorithm,	ļ
Modular arithmetic, Groups, Rings and Fields.	ļ
(Text 1: Chapter 1- 1, 2 & 3, Chapter 3- 2, 3 & 4)	
Module-2	8 Hours
Block Ciphers and Data Encryption Standard (DES): Traditional Block	L2, L3
Cipher structure, Data encryption standard (DES).	ļ
Advanced Encryption Standards: The AES structure, AES transformation	
function, AES key expansion. (Text 1: Chapter2- 1&2, Chapter 4-2, 3 & 4)	
Module-3	8 Hours
Public Key Cryptography and RSA: Principles of Public-Key	L2, L3
Cryptosystems, The RSA algorithm, Diffie-Hellman Key Exchange, Elgamal	ļ
cryptographic system, Elliptic Curve Cryptography. (Text 1: Chapter 8-1	ļ
& 2, Chapter 9- 1, 2 & 4)	
Module-4	8 Hours
Pseudo-Random-Sequence Generators and Stream Ciphers: Linear	L2, L3
Congruential Generators, Linear Feedback Shift Registers, Design and	
analysis of stream ciphers, Stream ciphers using LFSRs- Geffe Generator,	
Generalized Geffe Generator, Beth-Paper stop-and-go generator.	
One-Way Hash Functions: Background- Length of One-Way Hash	
Functions, Overview of One-Way Hash Functions, MD4, MD5. (Text 2:	
Chapter 16- 16.1 to 16.4, Chapter 18- 18.1, 18.4 & 18.5)	
Module-5	8 Hours
Message Authentication Codes: Message Authentication requirements,	L2, L3
Message Authentication Functions, Security of MACs, MACs Based on	
Block Ciphers: DAA and CMAC.	
Digital Signatures: Digital Signatures, NIST Digital Signature Algorithm.	
(Text 1: Chapter 11- Section 1, 2, 4 & 6, Chapter 12- Section 1, 4)	

CO1	Apply classical cryptographic algorithms to encrypt and decrypt the data using											
	number theory concepts.											
CO2	Explore symmetric cryptographic algorithms to encrypt and decrypt the											
	information.											
CO3	Apply asymmetric cryptographic algorithms to encrypt and decrypt the											
	information.											
CO4	Explore pseudo random sequence generators and one-way hash functions.											
CO5	Analyze message authentication codes and digital signature techniques.											

Textbooks:

- 1. William Stallings, Cryptography and Network Security Principles and Practice, Pearson Education Inc., 6th edition, 2014.
- 2. Bruce Schneier, Applied Cryptography Protocols, Algorithms, and Source code in C, Wiley Publications, 2nd edition.

Reference Books:

- 1. Behrouz A. Forouzan, Cryptography and Network Security, TMH, 2007.
- 2. AtulKahate, Cryptography and Network Security, TMH, 2003.

MOOCs:

https://digimat.in/nptel/courses/video/106105031/L01.html

https://onlinecourses.nptel.ac.in/noc22_cs03/

https://archive.nptel.ac.in/courses/106/107/106107155/

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	Grand Total		100

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	1	-	1	-	-
CO2	3	2	-	-	-	-	-	-	-	1	-	1	-	-
CO3	3	2	-	-	-	-	-	-	_	1	-	1	-	-
CO4	3	2	-	-	-	-	-	-	-	1	-	1	-	-
CO5	3	2	-	-	-	-	-	-	-	1	-	1	-	-
Average	3	2	-	-	-	-	-	-	-	1	-	1	-	-

Low-1: Medium-2: High-3



SEMESTER –VII Program Elective-3

Course: Machine Learning with Python

Course Code	22ECE742	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites:

Course Objectives: Students will be taught;

CLO1	Machine learning concepts and problems relevant to machine learning.
CLO2	Representation of Decision Tree for the decision learning problem.
CLO3	Neural Networks applications in machine learning.
CLO4	Bayes classifier and K NN algorithm.
CLO5	Statistical analysis of machine learning problems.

Content	No. of Hours / RBT levels
Module 1	8 Hours
Introduction: Well posed learning problems, Designing a Learning System, respective and Issues in Machine Learning.	L1, L2,
Concept Learning : Concept Learning Task, Concept Learning as search, Find S algorithm, Vector space, Candidate Elimination algorithm. Python programs using NumPy, and Matplotlib. (Text-1:1.1 to 1.3, 2.2 to 2.5)	
Module 2	8 Hours
Decision Tree Learning: Decision Tree representation, Appropriate problems for decision learning Basic Decision tree algorithm, hypothesis space search in decision tree learning, Issues in decision tree learning. Python programs on Decision tree. (Text-1:3.2 to 3.5 & 3.7)	L2, L3
Module 3	8 Hours
Artificial Neural Networks: Introduction, Neural Network Representation, Appropriate problems, Perceptrons, Back Propagation algorithm. Numerical. Examples, Python Examples on ANN. (Text-1: 4.1, 4.2, 4.3, 4.4, 4.5 & 4.6)	L1, L2,
Module 4	8 Hours
Bayesian Learning: Introduction, Bayes Theorem, Bayes and Concept Learning, ML and LS error hypothesis, ML for predicting probabilities, ML for predicting probabilities Naïve Bayes classifier, Bayesian belief networks. Numerical examples. Python examples on Naïve Bayes Classifier. (Text-1:6.1 to 6.5, 6.9 & 6.11)	L2, L3
Module 5	8 Hours
Instance Based Learning: Introduction, k-nearest neighbor learning, locally weighted regression, radial basis function, Numerical examples on KNN, Python programs on KNN. (Text 1:8.1 to 8.4) Reinforcement Learning: Introduction, Learning Task, Q- Learning: Q learning Algorithm. (Text 1:13.1 to 13.3)	L2, L3

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CO1	Understand the design of Learning System and Python Libraries used in Machine
	Learning.
CO2	Interpret the appropriate problems for Decision Tree Learning and solve with Python
	programming.
CO3	Describe the Artificial Neural Networks, Perceptrons and Back Propagation Algorithm.
CO4	Apply theory of probability to concept learning and Bayes Classifier.
CO5	Analyze Instance Based Learning and Reinforcement Learning.

TextBook:

- 1. Tom M. Mitchell, Machine Learning India Edition, McGraw Hill Education, 2013 **Reference Books:**
- 1. Anuradha Srinivasaraghavan and Vincy Joseph, Machine Learning, 2020, Wiley.
- 2. Aurelien Geron, Hands-on Machine Learning with Scikit-Learn and Tensor Flow, O'REILLY, 2017 Edition.
- 3. Fabio Nelli, Python Data Analytics, with Pandas, NumPy and Matplotlib Second Edition, 2018.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other.

The Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks		
	CIE Test-1	40			
CIE	CIE Test-2	40	50		
CIE	CIE Test-3	40	50		
	Assignments	10			
SEE	Semester End Examination	50	50		
	Grand Total		100		

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	1		-		-	-	-		-	2	1	1
CO2	2	2	1		1		-	1	-		-	2	1	1
CO3	3	1	1		ı		-	ı			-	2	1	1
CO4	2	2	1		-		-	-			-	2	1	1
CO5	2	2	1		-		-	-			-	1`	1	1
Average	2	2	1		-		-					2	1	1

Low-1: Medium-2: High-3

SEMESTER – VII Program Elective-3

Course: Optical Fiber Communication

Course Code	22ECE743	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Basic concepts of optical fiber Communication.
CLO2	Transmission characteristics and losses in optical fiber.
CLO3	Types of optical sources and detectors
CLO4	Optical components and its applications in optical communication networks
CLO5	Network standards in optical fiber and Network architectures along with its functionalities.

Content	No. of Hours / RBT levels
Module 1	8 Hours
Optical fiber communications : Historical development, The general system, Advantages of optical fiber communication.	L3
Optical fiber wave guides : Ray theory transmission, Modes in planar guide, Phase and group velocity.	
Cylindrical fiber: Modes, Step index fibers, Graded index fibers, Single mode fibers. (Text 2: 1.1 to 1.3, 2.2, 2.3.2, 2.3.32.4 & 2.5)	
Module 2	8 Hours
Transmission characteristics of optical fibers: Attenuation, Material absorption losses, Linear scattering losses, Nonlinear scattering losses, Fiber bend loss, Dispersion and intramodal dispersion. Optical Fiber Connectors: Fiber alignment and joint loss. Fiber splices: Fusion Splices, Mechanical splices, Cylindrical ferrule connectors, Duplex and Multiple fiber connectors. Fiber couplers: Three and four port couplers, star couplers and Wavelength division multiplexing couplers. (Text 2: 3.1 to 3.9, 5.2, 5.3 & 5.6)	L3
Module 3	8 Hours
Optical sources: Light Emitting diodes, LED Structures, Light Source Materials, Quantum Efficiency and LED Power, Modulation. (Text 1:4.2.1 to 4.2.4) Laser Diodes: Modes and Threshold conditions, Laser diode Rate equation, External Quantum Efficiency and Resonant Frequencies. (Text 1: 4.3.1 to 4.3.4) Photodetectors: Physical principles of Photodiodes, Photo detector noise and Detector response time. (Text 1: 6.1 to 6.3)	L3
Module 4	8 Hours
WDM Concepts and Components : Operational Principles of WDM, Mach-Zehnder Interferometer Multiplexers, Fiber grating filters, Tunable sources. (Text 1: 10.1.1, 10.2.5, 10.4 & 10.9)	L3

Je.

Optical amplifiers: Basic application and Types, Semiconductor optical	
amplifiers and Erbium Doped Fiber Amplifiers (Text 1: 11.1 to 11.3)	
Module 5	8 Hours
Optical Networks: Network Concepts, Network Topologies, SONET/SDH,	L3
High Speed Lightwave Links, Optical Add/Drop Multiplexing and optical	
switching. (Text 1: 13.1 to 13.6)	

CO1	Explain the concept of optical fiber communication
CO2	Describe the transmission characteristics and losses, Couplers and connectors in
COZ	optical fiber communication
CO3	Describe the constructional features and the characteristics of optical sources and
COS	detectors.
CO4	Discuss the principle of WDM and its Components.
CO5	Illustrate Optical network concepts and its switching.

Textbooks:

- 1. Gerd Keiser, Optical Fiber Communication, 5th edition, McGraw Hill Education(India) Private Limited, 2015.
- 2. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010.

Reference Book:

1. Joseph C Palais, Fiber Optic Communication, 5th edition, Pearson Education, 2009.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	50
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	Grand Total		100



					CO-	PO aı	nd PS	О Ма	pping					
CO/PO	PO1	P02	PO3	P04	PO5	P06	PO7	P08	P09	PO10	PO11	PO12	PSO1	PS02
CO1	3	2	1	-	-	-	-	-	-	-	-	3	2	2
CO2	3	2	1	-	-	-	-	-	-	-	-	3	2	2
CO3	3	2	1	-	-	-	-	-	-	-	-	3	2	2
CO4	3	2	1	-	-	-	-	-	-	-	-	3	2	2
CO5	3	2	1	-	-	-	_	-	-	-	-	3	2	2
Average	3	2	1	-	-	-	-	-	-	-	-	3	2	2

Low-1: Medium-2: High-3

SEMESTER – VII Program Elective-3

Course: Biomedical Signal Processing

Course Code	22ECE744	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Different types of biomedical signals.
CLO2	Processing of biomedical signals.
CLO3	Data compression techniques.
CLO4	Methods of analysis of ECG signals.
CLO5	Analysis of EEG signals

Content	No. of Hours / RBT levels
Module-1	8 Hours
Introduction to Biomedical Signals: The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis.	L2, L3
Electrocardiography : Basic electrocardiographies, ECG lead systems, ECG signal characteristics.	
Signal Conversion: Simple signal conversion systems, Conversion requirements for biomedical signals, Signal conversion circuits (Text 3: chapter 1,Text 1: chapter 2,chapter 3)	
Module-2	8 Hours
Signal Averaging: Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging. Adaptive Noise Cancelling: Principal noise canceller model, 60-Hzadaptive cancelling using a sine wave model, other applications of adaptive filtering. (Text 1: chapter 9 and chapter 8) Module-3	L2, L3 8 Hours
Data Compression Techniques: Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding, data reduction algorithms The Fourier transform, Correlation, Convolution, Power spectrum estimation, Frequency domain analysis of the ECG. (Text 1)	L2, L3
Module-4 Cardiological signal processing: Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor. (Text 1: chapter 12, chapter 11)	8 Hours L2, L3

Module-5	8 Hours
Neurological signal processing: The brain and its potentials, The	L2, L3
electrophysiological origin of brain waves, The EEG signal and its	
characteristics (EEG rhythms, waves, and transients), Correlation.	
Analysis of EEG channels: Detection of EEG rhythms, Template matching	
for EEG, spike and wave detection(Text 2 and 3)	

CO1	Analyze the various biomedical signals.
CO2	Apply signal averaging and adaptive signal processing to extract biomedical signals
	from noise.
CO3	Apply classical and modern filtering and compression techniques for ECG and EEG
	signals.
CO4	Explain the basics of ECG and its parameters.
CO5	Describe the detection of EEG signals

Textbooks:

- 1. Willis J. Tompkins, Biomedical Digital Signal Processing, PHI 2001.
- 2. D C Reddy, Biomedical Signal Processing Principles and Techniques, McGraw-Hill publications, 2005.
- 3. Rangaraj M. Rangayyan, Biomedical Signal Analysis, John Wiley & Sons 2002.

MOOCs:

https://www.classcentral.com/course/swayam-biomedical-signal-processing-10069. https://onlinecourses.nptel.ac.in/noc20 ee41/preview.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses.

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50

12.

	CO-PO and PSO Mapping													
CO/PO	P01	P02	P03	PO4	P05	P06	P07	P08	P09	PO10	PO11	PO12	PS01	PS02
CO1	3	3	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-	2	-
CO3	3	-	-	-	-	-	-	-	-	-	-	1	-	1
CO4	3	3	-	-	-	-	-	-	-	-	-	1	2	-
CO5	3	1	-	1	-	-	-	-	-	1	-	1	2	1
Average	3	3	-	-	-	_	-	-	-	-	-	1	2	1

Low-1: Medium-2: High-3

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SEMESTER – VII Open Elective-2 (Offered to other than ECE students)

Course: Wireless and Mobile Networks

Course Code	22ECE751	CIE Marks	50
Hours/Week (L: T: P)	3: 0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Digital Communication, Spread Spectrum Modulation.

Course Learning Objectives: Students will be taught.

CLO1	Fundamental concept of wireless communication.
CLO2	Wireless Body Area Networks and Personal Area networks
CLO3	Standards and Architecture of Wireless Local Area Networks.
CLO4	Architecture, protocols of WMANs and WWANs
CLO5	Types of Adhoc Networks, Protocols and Applications.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Fundamentals of Wireless Communication: Wireless Communication	L2, L3
System, Wireless Media, Frequency Spectrum, Wireless Communication	
Channel Specifications, Types of Wireless Communication Systems. Text1:	
1.1, 1.2, 1.3, 1.4, 1.6 & 1.7	
Basics of Wireless Networks: Introduction, Wireless Network, Wireless	
Switching Technology, Wireless Communication Problems, Wireless	
Network Reference Model, Wireless Networking Issues, Wireless	
Networking Standards.Text1: 2.1, 2.2, 2.3, 2.4 & 2.5	
Module-2	8 Hours
Wireless Body Area Networks: Wireless Body Area Network (WBAN),	L2, L3
Network Architecture, Network Components, Design Issues, Network	
Protocols, WBAN Technologies. Text1:3.1, 3.3, 3.4, 3.5, 3.6 & 3.7.	
Wireless Personal Area Networks: Wireless Personal Area Network	
(WPAN), Network Architecture, WPAN Components, WPAN Technologies	
and Protocols, WPAN Applications. Text 1:4.1, 4.2, 4.3 & 4.5	
Module-3	8 Hours
Wireless Local Area Networks: Network Components, Design	L2, L3
Requirements of WLAN, Network Architecture, WLAN Standards, IEEE	
802.11p, WLAN Applications.Text1:5.1, 5.2, 5.3, 5.4, 5.6 & 5.7.	
Module-4	8 Hours
Wireless Metropolitan Area Networks: Wireless Metropolitan Area	L2, L3
Networks, WMAN Network Architecture, Network Protocols, Broadband	
Wireless Networks, WMAN Applications. Text1:6.1,6.2,6.3,6.4,6.5	
Wireless Wide Area Networks: Cellular Networks, WLAN versus WWAN,	
WWAN Applications. Text1:7.1, 7.3 &7.5	
Module-5	8 Hours
Wireless Ad Hoc Networks: Wireless Ad Hoc Networks, Mobile Ad Hoc	L2, L3
Networks, Wireless Sensor Networks, Wireless Mesh Networks, Vehicular	
Ad Hoc Networks (VANETs)	
Text1: 8.1, 8.2, 8.3, 8.4 & 8.5	

CO1	Understand Wireless communication, fundamentals, communication systems, and
	networks.
CO2	Discuss the operation of WPAN components, standards and protocols.
CO3	Describe the various protocols and standards (WiMAX) used in WMAN, broadband
	wireless networks – LMDS, MMDS.
CO4	Demonstrate the communication protocols and interworking of WLAN, WMAN and
	WWAN
CO5	Illustrate the concept of wireless ad hoc networks, the architecture and protocols
	and the applications of wireless ad hoc networks

Textbook:

1. Sunil Kumar S Manvi, Mahabaleshwar S Kakkasageri, Wireless and Mobile Networks, 2nd Edition, Wiley India Pvt. Ltd. 2016.

Reference books:

1. Imrich Chlamtac Yi-Bang Lin, Wireless and Mobile Network Architectures, Wiley Publication, 2008.

Software/Learning Websites:

- 1. www.philadelphia.edu.jo/newlibrary/./file101fc6e5c77f4675b2958dc10a8c99c9 pdf
- 2. www.radio Electronics.com/info/wireless/Bluetooth/Bluetooth overview.php
- 3. www.gsma.com/futurenetworks/wp-content/uploads/2014
- 4. www.octoscope.com/English/.../octoscope_WirelessTutorial 20090209 pdf.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	Ε0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50

	CO-PO and PSO Mapping													
CO/PO	PO1	P02	PO3	P04	PO5	P06	P07	P08	P09	PO10	PO11	PO12	PS01	PS02
CO1	2	1	1							2	2	2	1	1
CO2	2	1	1							2	2	2	1	1
CO3	2	1	1							2	2	2	1	1
CO4	2	1	1							2	2	2	1	1
CO5	2	1	1							2	2	2	1	1
Average	2	1	1							2	2	2	1	1

Low-1: Medium-2: High-3



SEMESTER – VII Open Elective-2 (Offered to other than ECE students)

Course: Automotive Electronics

Course Code	22ECE752	CIE Marks	50
Hours/Week (L: T: P)	3: 0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Basic Electronics, Elements Mechanical Engineering, Basic concepts of Physics.

Course Learning Objectives: Students will be taught;

CLO1	Basics of automotive systems and electronic control.				
CLO2	Sensors and Actuators				
CLO3	Digital Engine control features.				
CLO4	Networking of various modules in automotive systems and communication				
	protocols				
CLO5	Automotive Diagnostics				

Content	No. of Hours / RBT level
Module-1	8 Hours
Automotive Fundamentals Overview: Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System - Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Drive Train - Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System (Text 1) The Basics of Electronic Engine Control: Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Electronic Ignition. (Text 1)	L3
Module-2	8 Hours
Automotive Sensors: Automotive Control System applications of Sensors and Actuators –Variables to be measured, Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2/EGO) Lambda Sensors, (Text 1) Automotive Engine Control Actuators: Solenoid, Fuel Injector, EGR Actuator, Ignition System (Text 1)	L3
Module-3	8 Hours
Digital Engine Control Systems: Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control - Closed loop Ignition timing, Integrated Engine Control System -	L3

Secondary Air Management, Evaporative Emissions Canister Purge,	
Automatic System Adjustment, System Diagnostics. (Text 1)	
Control Units: Operating conditions, Design, Data processing,	
Programming, Digital modules in the Control unit, Control unit software.	
(Text 2)	
Module-4	8 Hours
1	
Automotive Networking: Bus Systems, Classification, Applications in the	L3
vehicle, Coupling of networks, Examples of networked vehicles	
CAN Bus: Protocol layers, Message format.	
LIN Bus: Overview, Applications.	
MOST Bus: Introduction, Requirements, Type of use.	
Bluetooth: Overview, Applications.	
Flex Ray: Overview, Areas of application. Diagnostic Interfaces. (Text 2)	
Vehicle Motion Control: Typical Cruise Control System, Digital Cruise	
Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise	
Control configuration, Cruise Control Electronics (Digital only), Antilock	
Brake System (ABS) (Text 1)	
Module-5	8 Hours
Automotive Diagnostics: Timing Light, Engine Analyzer, On-board	L3
diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection	
Systems – Accelerometer based Air Bag systems. (Text 1: Chapter 10)	
Future Automotive Electronic Systems: Collision Avoidance Radar	
warning Systems, Low tire pressure warning system, Heads Up display,	
Speech Synthesis, Navigation – Navigation Sensors – Radio Navigation,	
Signpost navigation, dead reckoning navigation, Voice Recognition Cell	
Phone dialing, Advanced Cruise Control, Stability Augmentation,	
Automatic driving Control.(Text 1)	

CO1	Acquire an overview of automotive components, subsystems, and basics of Electronic
	Engine Control in today's automotive industry.
CO2	Interfacing with microcontrollers / microprocessors during automotive system
	design.
CO3	Explain operation of Digital Engine Control Systems & Secondary air management in
	automobiles.
CO4	Describe the networking of various modules in automotive systems, Communication
	protocols and diagnostics of the sub systems.
CO5	Explain the electronics that attribute the reliability, safety, and smartness to the
	automobiles, providing add-on comforts

Textbooks:

- 1. William B. Ribbens, Understanding Automotive Electronics, 6th Edition, Elsevier Publishing, 2003.
- 2. Robert Bosch Gmbh, Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th Edition, John Wiley, 2007.

Reference Books:

- 1. Detlef E. Ricken and Wolfgang Gessner, vanced Microsystems for Automotive Applications, Springer Publishing, 1998.
- 2. Automotive Electronic Diagnostics (Course-2) Kindle Edition

MOOCs:

https://www.youtube.com/watch?v=IVBb6KJM1fk

https://www.youtube.com/watch?v=3E1SXG7VkQk

https://www.youtube.com/watch?v=Sh6qZ-Sh7Jk

https://www.youtube.com/watch?v=LZ82iANWBL0

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50

	CO/PO and PSO Mapping													
CO/PO	PO1	P02	PO3	P04	PO5	P06	P07	P08	P09	PO10	PO11	PO12	PSO1	PS02
CO1	3	2	1			2	1	1				2	2	1
CO2	3	2	1			2	1	1				2	2	1
CO3	3	2	1			1	1	2				2	2	1
CO4	3	2	1			2	1	2				2	2	1
CO5	3	2	1			2	1	2				1	2	1
Average	3	2	1			2	1	2				2	2	1

Low-1: Medium-2: High-3

SEMESTER –VII Open Elective-2 (Offered to other than ECE students)

COURSE: Basic VLSI Design

Course Code	22ECE753	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Digital System Design.

Course Learning Objectives: Students will be taught.

CLO1	Fabrication and Electrical Properties of MOS devices
CLO2	VLSI design process and design rules.
CLO3	Basic Electrical Properties of MOS and BiCMOS Circuits.
CLO4	MOS and BiCMOS Circuit Design Processes.
CLO5	Subsystem Design for VLSI.

Content	No. of Hours / RBT levels
Module 1	8 Hours
Introduction: Moore's law, speed power performance, nMOS fabrication, CMOS fabrication: n-well processes, BiCMOS, Comparison of bipolar and CMOS. Drain to source current versus voltage characteristics, threshold voltage, transconductance. (Text-1: 1.1, 1.8, 1.8.2, 1.10, 2.1, 2.2 & 2.3)	L3
Module 2	8 Hours
Basic Electrical Properties of MOS and BiCMOS Circuits: nMOS inverter, Determination of pull up to pull down ratio: nMOS inverter driven through one or more pass transistors, alternative forms of pull up, CMOS inverter, BiCMOS inverters, latch up. Basic Circuit Concepts: Sheet resistance, area capacitance calculation, Delay unit, inverter delay, estimation of CMOS inverter delay, super buffers, BiCMOS drivers. (Text-1: 2.6, 2.7, 2.8, 2.9, 2.10, 2.12.3, 2.13, 4.1, 4.2, 4.5, 4.6, 4.7.1, 4.8.2 & 4.8.3)	L3
Module 3	8 Hours
MOS and BiCMOS Circuit Design Processes: MOS layers, stick diagrams, nMOS design style, CMOS design style Design rules and layout & Scaling of MOS Circuits: λ - based design rules, scaling factors for device parameters. (Text-1: 3.1, 3.2, 3.2.1, 3.2.2, 3.3, 5.1 & 5.2)	L3
	8 Hours
Module 4 Subsystem Design and Layout-1: Switch logic pass transistor, Gate logic inverter, NAND gates, NOR gates, pseudo nMOS, Dynamic CMOS Examples of structured design: Parity generator, Bus arbitration, multiplexers, logic function block, code converter.(Text-1: 6.2, 6.2.1, 6.3, 6.3.1, 6.3.3, 6.3.4.1, 6.3.4.2, 6.4, 6.4.2, 6.4.3 & 6.4.4)	L3
	8 Hours
Module 5 Subsystem Design and Layout-2: Clocked sequential circuits, dynamic shift registers, bus lines, General considerations, 4-bit arithmetic processes, 4-bit shifter, Regularity- Definition & Computation Practical	L3

aspects and testability: Some thoughts of performance, optimization and	
CAD tools for design and simulation.	
(Text-1: 6.5-6.5.3, 6.5.4, 7.1, 7.2, 7.2.1, 7.2.2, 8.1, 8.2, 10.1, 10.1.1, 10.11	
& 10.12)	

CO1	Identify the CMOS layout levels, and the design layers used in the process
	sequence.
CO2	Describe the general steps required for processing of CMOS integrated circuits.
CO3	Design static CMOS combinational and sequential logic at the transistor level.
CO4	Demonstrate different logic styles such as complementary CMOS logic, pass- transistor Logic, dynamic logic, etc.
CO5	Interpret the need for testability and testing methods in VLSI.

Text Book:

1. Douglas A Pucknell and Kamran Eshraghian, Basic VLSI Design, 3rd edition, Prentice Hall of India publication, 2005.

References:

- 1. Sung Mo (Steve) Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits, Analysis and Design, Tata McGraw Hill, 3rd edition, 2003.
- 2. S.M. Sze, VLSI Technology, 2nd edition, Tata McGraw Hill, 2003.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

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			Marks			
	CIE Test-1	40				
CIE	CIE Test-2	40	Ε0			
CIE	CIE Test-3	40	50			
	Assignments	10				
SEE	Semester End Examination	50	50			
	Grand Total					



	CO-PO and PSO Mapping													
CO/PO	P01	P02	P03	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PSO1	PS02
CO1	3	3	-	1	ı	-	-	-	1	1	ı	2		
CO2	3	3	-	-	1	1	-	1	3	2	1	2		
CO3	3	3	-	-	1	1	-	1	3	2	1	2		
CO4	3	3	-	-	1	1	-	1	3	2	1	2		
CO5	3	3	-	1	1	1	-	1	3	2	1	2		
Average	3	3	-	-	1	1	-	1	3	2	1	2		

Low-1: Medium-2: High-3



SEMESTER – VII Open Elective-2 (Offered to other than ECE students)

Course: Smart Sensors and Instrumentation

Course Code	22ECE754	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Understand various technologies associated in manufacturing of sensors
CLO2	Acquire knowledge about types of sensors used in modern digital systems
CLO3	Understand types of instrument errors and circuits for multirange Ammeters and Voltmeters.
CLO4	Describe principle of operation of digital measuring instruments and Bridges
CLO5	Understand the operations of transducers and Data Acquisition System.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Introduction to sensor-based measurement systems:	L2
General concepts and terminology, sensor classification, Primary Sensors,	
material for sensors, microsensor technology. (Text 1:1.1, 1.2, 1.7-1.9)	
Module-2	8 Hours
Self-generating Sensors- Thermoelectric sensors, piezoelectric sensors,	L2
pyroelectric sensors, photovoltaic sensors, electrochemical sensors. (Text 1: 6.1 to 6.5)	
Module-3	8 Hours
Principles of Measurement: Performance characteristics, Static Characteristics, Error in Measurement, Types of Static Error, Multirange Ammeters, Multirange voltmeter. Digital Voltmeter: Ramp Technique, Dual slope, integrating Type DVM, and Successive Approximations type DVM.	L3
(Text 2: 1.2 -1.6, 3.2, 4.4, 5.2-5.4, 5.6)	
Module-4	8 Hours
Digital Instruments: Universal counter, Decade counter, Digital tachometer, Digital pH meter, Digital phase meter. Bridges: Wheatstone's Bridge, AC Bridges - Capacitance and Inductance Comparison bridge, Wien's bridge.(Text2: 6.5, 6.6, 6.9, 6.10, 6.12, 11.2, 11.8 -11.10 & 11.14)	L3
Module-5	8 Hours
Transducers: Introduction, Electrical Transducer, Selecting a Transducer Resistive Transducer, Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT. Data Acquisition System (DAS) : Introduction, Objectives of DAS, Signal conditioning of inputs, Single channel DAS, Computer based DAS. (Text2: 13.1-13.8, 13.11, 17.1-17.4 & 17.6).	L2



CO1	Understand the concept of Sensors and its manufacturing.
CO2	Describe the operation of various self-generating sensors.
CO3	Discuss the operation of measurements and the operation of Digital voltameter.
CO4	Evaluate various measurement parameters using digital multimeter and bridges.
CO5	Elaborate the working of transducers and Data Acquisition System.

Textbooks:

- 1. Sensors and Signal Conditioning, Ramon Pallas Areny, John G. Webster, 2nd edition, John Wiley, and Sons, 2000.
- 2. Electronic Instrumentation, H.S.Kalsi, Mc Graw Hill, 3rdEdition, 2012.

Reference Books:

- 1. Electronic Instrumentation & Measurements, David Bell, Oxford University Press PHI, 2ndEdition, 2006.
- 2. Modern Electronic Instrumentation and Measuring Techniques, D. Helfrick and W.D. Cooper Pearson, 1stEdition, 2015.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	Grand Total		100

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	-	-	-	-	-	-	-	-	-	-	1	-
CO2	1	1	1	ı	-	ı	-	-	-	-	ı	-	1	1
CO3	1	2	-	-	-	-	-	-	-	-	-	1	1	-
CO4	3	3	2	-	-	-	-	1	-	-	-	1	2	1
CO5	2	1	-	-	-	-	-	1	-	-	-	1	2	1
Average	2	2	-	-	-	-	-	1	-	-	-	1	2	1

Low-1: Medium-2: High-3

SEMESTER - VII

Course: Project Phase-1

Course Code	22ECEP76	CIE Marks	100
Hours/Week (L: T: P)	2 hr/week	SEE Marks	
No. of Credits	2	Examination Hours	

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student or to a group having not more than 4 students. In extraordinary cases, like the funded projects requiring students from different disciplines, the project student strength can be 5 or 6.

CIE procedure for Project Work Phase - 1:

- (i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide. The CIE marks awarded for the project work phase -1, shall be based on the evaluation of the project work phase -1 Report (covering Literature Survey, Problem identification, Objectives and Methodology), project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the Project report shall be the same for all the batch mates.
- (ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

SEMESTER -VIII

Course: Cellular and Mobile Communication

Course Code	22ECE81	CIE Marks	50
Hours/Week (L:T:P)	4:0:0	SEE Marks	50
No. of Credits	4	Examination Hours	03

Prerequisites: Communication Systems

Course Learning Objectives: Students will be taught;

CLO1	Fundamentals of wireless communication.
CLO2	Multicarrier concepts and synchronization for LTE communication.
CLO3	Multiple Access and channel structure of LTE.
CLO4	Resource allocation and scheduling procedure at physical layer.
CLO5	Data Flow, Radio Resource Management and Mobility Management in LTE.

Content	No. of Hours/ RBT levels
Module-1	8 Hours
Wireless Fundamentals: Communication System Building Blocks, The	L1, L2, L3
Broadband Wireless Channel: Path Loss and Shadowing- Path Loss,	L1, L2, L3
Shadowing, Cellular Systems- The Cellular Concept, Analysis of Cellular	
Systems, Sectoring, The Broadband Wireless Channel: Fading-Delay	
Spread and Coherence Bandwidth, Doppler Spread and Coherence Time,	
Angular Spread and Coherence Distance. (Text-1: 2.1, 2.2.1, 2.2.2, 2.3.1,	
2.3.2, 2.3.3, 2.4.1, 2.4.2 & 2.4.3).	
Module-2	8 Hours
Multicarrier Modulation: The Multicarrier Concept- An Elegant Approach	L1, L2, L3
to Inter symbol Interference, OFDM Basics-Block Transmission with Guard	, ,
Intervals, Circular Convolution and the DFT, The Cyclic Prefix, Frequency	
Equalization, An OFDM Block Diagram, OFDM in LTE, Timing and	
Frequency Synchronization- Timing Synchronization, Frequency	
Synchronization. (Text-1: 3.1.1, 3.2.1, 3.2.2, 3.2.3, 3.2.4, 3.2.5, 3.3, 3.4.1 &	
3.4.2)	
Frequency Domain Multiple Access: OFDMA and SC-FDMA	
Multiple Access for OFDM Systems- Multiple Access Overview, Random	
Access vs. Multiple Access, Frequency Division Multiple Access (OFDM-	
FDMA), Time Division Multiple Access (OFDM-TDMA), Code Division	
Multiple Access (OFDM-CDMA or MC-CDMA). (Text-1: 4.1.1, 4.1.2, 4.1.3,	
4.1.4 & 4.1.5).	
Module-3	8 Hours
Orthogonal Frequency Division Multiple Access (OFDMA)- OFDMA: How It	L1, L2, L3
Works, OFDMA Advantages and Disadvantages, Single-Carrier Frequency	
Division Multiple Access (SC-FDMA)- SC-FDMA: How It Works, SC-FDMA	
Advantages and Disadvantages. (Text-1: 4.2.1, 4.2.2, 4.3.1 & 4.3.2).	
Overview and Channel Structure of LTE: Introduction to LTE- Design	
Principles, Network Architecture, Radio Interface Protocols, Hierarchical	
Channel Structure of LTE- Logical Channels: What to Transmit, Transport	
Channels: How to Transmit, Physical Channels: Actual Transmission,	
Channel Mapping. (Text-1: 6.1.1, 6.1.2, 6.1.3 6.2.1, 6.2.2, 6.2.3 & 6.2.4).	

Module-4	8 Hours
Downlink OFDMA Radio Resources- Frame Structure, Physical Resource	L1, L2, L3
Blocks for OFDMA, Resource Allocation, Supported MIMO Modes, Uplink	
SC-FDMA Radio Resources- Frame Structure, Physical Resource Blocks for	
SC-FDMA, Resource Allocation, Supported MIMO Modes. (Text-1: 6.3.1,	
6.3.2, 6.3.3, 6.3.4, 6.4.1, 6.4.2, 6.4.3 & 6.4.4).	
Physical Layer Procedures and Scheduling: Hybrid-ARQ Feedback- H-ARQ	
Feedback for Downlink (DL) Transmission, H-ARQ Indicator for Uplink (UL)	
Transmission, Cell Search, Random Access Procedures. (Text-1: 9.1.1,	
9.1.2, 9.8 & 9.9).	
Module-5	8 Hours
Module-5 Data Flow, Radio Resource Management, and Mobility Management:	8 Hours L1, L2, L3
Data Flow, Radio Resource Management, and Mobility Management:	
Data Flow, Radio Resource Management, and Mobility Management: PDCP Overview- Header Compression, Integrity and Ciphering, MAC/RLC	
Data Flow, Radio Resource Management, and Mobility Management: PDCP Overview- Header Compression, Integrity and Ciphering, MAC/RLC Overview- Data Transfer Modes, Purpose of MAC and RLC Layers, PDU	
Data Flow, Radio Resource Management, and Mobility Management: PDCP Overview- Header Compression, Integrity and Ciphering, MAC/RLC Overview- Data Transfer Modes, Purpose of MAC and RLC Layers, PDU Headers and Formats, ARQ Procedures, RRC Overview- RRC States, RRC	
Data Flow, Radio Resource Management, and Mobility Management: PDCP Overview- Header Compression, Integrity and Ciphering, MAC/RLC Overview- Data Transfer Modes, Purpose of MAC and RLC Layers, PDU Headers and Formats, ARQ Procedures, RRC Overview- RRC States, RRC Functions, Mobility Management- S1 Mobility, X2 Mobility, RAN	

CO1	Explain the concepts of broadband wireless channels and cellular systems.
CO2	Explain the concepts of OFDM in LTE and its synchronization.
CO3	Explain the concepts of OFDMA, SCFDMA and channel structure of LTE.
CO4	Explain the concepts of Resource allocation and scheduling procedure at physical layer.
CO5	Explain the concepts of Data Flow, Radio Resource Management, and Mobility Management in LTE.

Textbooks:

1. Fundamentals of LTE, Arunabha Ghosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, Pearson education (Formerly Prentice Hall, Communications Engg and Emerging Technologies), ISBN-13: 978-0-13-703311-9.

Reference Books:

- 1. Wireless Communications: Principles and Practice, Theodore Rappaport, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0- 13-042232-0.
- 2. LTE for UMTS Evolution to LTE-Advanced, Harri Holma and Antti Toskala, Second Edition 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003. 2



	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1										1	1
CO2	3						1				1		1	1
CO3	3						1				1		1	1
CO4	3											1		
CO5	3											1		1
Average	3	2	1				1				1	1	1	1

Low-1: Medium-2: High-3

SEMESTER -VIII Program Elective - 4

Course: Network and Cyber Security

Course Code	22ECE821	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Concepts of computer and network security.
CLO2	Transport-Level Security protocols.
CLO3	Electronic-Mail Security and IP Security protocols.
CLO4	Various Malicious software, Intruders and Firewall configurations.
CLO5	Cyber security issues and cyber anti patterns.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Computer and Network Security Concepts: Computer security concepts, OSI Security Architecture, Security attacks, security Services, Security mechanisms, Fundamental Security Design Principles, Attack Surfaces and Attack Trees, Model for network security, Standards. (Text-1: Chapter 1)	L3
Module-2	8 Hours
Transport-Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH). (Text-1: Chapter 17)	L3
Module-3	8 Hours
Electronic-Mail Security: Internet Mail Architecture, Email Threats and Comprehensive Email Security, S/MIME. (Text-1: Chapter 19: 19.1, 19.3, 19.4)	L3
IP Security: IP security overview, IP Security Policy, Encapsulation Security Payload (ESP) (Text-1: Chapter 20: 20.1, 20.2, 20.3)	
Module-4	8 Hours
Malicious Software: Types of Malicious Software, Advanced persistent threat. (Text 1: Chapter 21: 21.1, 21.2 Online Chapters) Intruders: Intruders, Intruder Detection (Text 1: Chapter 22: 22.1, 22.2 Online Chapters) Firewalls: Need for Firewalls, Firewall Characteristics and Access Policy, Types of Firewalls. (Text 1: Chapter 23: 23.1, 23.2, 23.3 Online Chapters)	L3
Module-5	8 Hours
Legal and Ethical Aspects: Cyber-crime and Computer Crime, Intellectual Property, Privacy, Ethical Issues. (Text 1: Chapter 24: 24.1, 24.2, 24.3, 24.4 Online Chapters) The Problems: Cyber Antipatterns: Antipatterns concept, Forces in Cyber antipatterns, Cyber antipattern templates, Micro antipattern templates, Full cyber antipattern template and Cyber security antipattern Catalog. (Text 2: Chapter 2)	L2

CO1	Explore Computer and network security concepts.
CO2	Analyze Transport-Level Security protocols.
CO3	Describe Electronic-Mail Security and IP Security.
CO4	Explore the types of Malicious software, Intruders and Firewall configurations.
CO5	Realize legal and ethical aspects in cyber security and Cybercrime with antipattern
COS	concepts.

Textbooks:

- 1. William Stallings, Cryptography and Network Security, Principles and Practice, 7th Edition, Pearson Education, 2010.
- 2. Thomas J. Mowbray, Cyber Security, John Wiley and Sons, 1st Edition 2013.

Reference Books:

- 1 Behrouz Forouzan, Cryptography and Network Security, TMH, 2007.
- 2 Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone, Handbook of AppliedCryptography, CRC press, reprint 2001.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses.

rable 1. Plotting thought to the Strategy for the distance of the Strategy for the Strategy				
	Component	Marks	Total	
			Marks	
	CIE Test-1	40		
CIE	CIE Test-2	40	F0	
CIE	CIE Test-3	40	50	
	Assignments	10		
SEE	Semester End Examination	50	50	

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	P04	PO5	P06	P07	PO8	P09	PO10	PO11	PO12	PSO1	PS02
CO1	1	2	-	2	-	-	-	-	-	-	1	1	2	2
CO2	2	2	-	2	-	-	-	-	-	-	1	1	2	2
CO3	2	2	-	2	-	-	-	-	-	-	1	1	2	2
CO4	2	2	-	2	-	-	-	-	-	-	1	1	2	2
CO5	2	2		2							1	1	2	2
Average	2	2	-	2	-	-	-	-	-	-	1	1	2	2

Low-1: Medium-2: High-3

SEMESTER -VIII Program Elective - 4

Course: DSP Algorithms and Architecture

Course Code	22ECE822	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	Introduction to Digital Signal Processing.
CLO2	Architectures for Programmable Digital Signal – Processing Devices.
CLO3	Programmable Digital Signal Processors.
CLO4	Implementation of Basic DSP Algorithms.
CL05	Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices.

Content	No. of Hours / RBT levels
Module-1	-
Introduction to Digital Signal Processing: Introduction, A Digital Signal –	8 Hours
Processing System, The Sampling Process, Discrete Time Sequences, Discrete	L2
Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-	
Invariant Systems, Digital Filters, Decimation and Interpolation.	
Computational Accuracy in DSP Implementations: Number Formats for	
Signals and Coefficients in DSP Systems, Dynamic Range and Precision,	
Sources of Error in DSP Implementation.	
Text-1: 2.1-2.6, 3.1-3.4	
Module-2	8 Hours
Architectures for Programmable Digital Signal – Processing Devices:	L3
Introduction, Basic Architectural Features, DSP Computational Building	
Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address	
Generation Unit, Programmability and Program Execution, Speed Issues,	
Features for External Interfacing.	
Text 1: 4.1-4.9	
Module-3	8 Hours
Programmable Digital Signal Processors: Introduction, Commercial Digital	L3
Signal-processing Devices, Data Addressing Modes of TMS32OC54XX,	
Memory Space of TMS32OC54xx Processors, Program Control. Detail Study	
of TMS320C54X & 54xx Instructions and Programming, On-Chip	
Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of	
TMS32OC54xx Processor.	
Text 1: 5.1-5.10	
Module-4	8 Hours
Implementation of Basic DSP Algorithms: Introduction, The Q – notation,	L3
FIR Filters, IIR Filters, Interpolation and Decimation Filters.	
Implementation of FFT Algorithms: Introduction, An FFT Algorithm for DFT	
Computation, Overflow and Scaling, Bit – Reversed Index. Generation and Implementation on the TMS32OC54xx.	
· ·	
Text 1:7.1-7.6, 8.1-8.6	

Je.

Module-5	8 Hours
Interfacing Memory and Parallel I/O Peripherals to Programmable DSP	L3
Devices: Introduction, Memory Space Organization, External Bus Interfacing	
Signals. Memory Interface, Parallel I/O Interface, Programmed I/O,	
Interrupts and I/O Direct Memory Access (DMA).	
Interfacing and Applications of DSP Processors: Introduction, Synchronous	
Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry	
Receiver, A Speech Processing System, An Image Processing System.	
Text 1:9.1-9.8, 11.1-11.5	

	<u>'</u>
CO1	Comprehend the knowledge and concepts of digital signal processing
COI	techniques.
CO2	Apply the knowledge of DSP computational building blocks to achieve speed in DSP
CO2	architecture or processor
CO3	Explain various types of Programmable Digital Signal Processors
CO4	Describe basic DSP algorithms using DSP processors
COF	Discuss synchronous serial interface and multichannel buffered serial port of DSP
CO5	device and the programming of CODEC interfacing.

Text books:

1. Avatar Singh and S. Srinivasan, Digital Signal Processing, Thomson Learning, 2010.

Reference books:

- 1. Digital Signal Processing: A practical approach, Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
- 2. Digital Signal Processors, B Venkataramani and M Bhaskar, TMH, 2nd Edition, 2010.
- 3. Architectures for Digital Signal Processing, Peter Pirsch John Weily, 2008.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	Ε0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	Grand Total		100



	CO-PO and PSO Mapping													
COs	PO1	P02	PO3	P04	P05	P06	P07	P08	P09	PO10	PO11	PO12	PSO1	PS02
CO1	1	2	-	2	-	-	-	-	-	-	1	1	2	2
CO2	2	2	-	2	-	-	-	-	-	-	1	1	2	2
CO3	2	2	-	2	-	-	-	-	-	-	1	1	2	2
CO4	2	2	-	2	-	-	-	-	-	-	1	1	2	2
CO5	2	2		2							1	1	2	2
Average	2	2	-	2	-	-	-	-	-	-	1	1	2	2

Low-1: Medium-2: High-3



SEMESTER -VIII Program Elective - 4

Course: ASIC Design

Course Code	22ECE823	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Analog Electronic Circuits, Design and Analysis of Digital Circuits, VLSI Design and Advanced VLSI.

Course Learning Objectives: Students will be taught;

CLO1	Application specific integrated circuits and its types.
CLO2	Programmable ASIC Logic cells and I/O cells.
CLO3	Low-level design entry and construction of ASIC using CAD tools.
CLO4	Algorithms used in Floor planning and Placement.
CLO5	Routing algorithms.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Introduction to ASICs: Types of ASICs, Full-Custom ASICs, Standard-Cell-	L2, L3
Based ASICs, Gate Array Based ASICs, Channelless Gate Array, Structured	
Gate Array, Programmable Logic Devices, Field-Programmable Gate	
Arrays, Design flow. ASIC cell libraries. Text Book 1 (Chapter1: 1.1 to	
1.1.8, 1.2, 1.5) CMOS Logic: Multipliers (Booth encoding), I/O calls, Call Compilers	
CMOS Logic: Multipliers (Booth encoding), I/O cells, Cell Compilers. (Text Book 1: Chapter2: 2.6.4, 2.7, 2.8)	
Module-2	8 Hours
Programmable ASIC Logic Cells: ACT 1 logic Module, Multiplexer logic as	L2, L3
function generators. Xilinx LCA: XC3000 CLB, Altera FLEX and Altera MAX.	
(Text Book 1: Chapter 5: 5.1.1, 5.1.3, 5.2.1, 5.3, 5.4)	
Programmable ASIC I/O Cells: Xilinx I/O Block, Boundary Scan, Other I/O	
Cells. (Text Book 1: Chapter 6: 6.7, 6.7.1, 6.8)	
Module-3	8 Hours
Low-Level Design Entry: Schematic entry: Hierarchical design, The cell	L2, L3
library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for	
ASICs and PCBs, Connections, Vectored Instances & Buses, Edit in place,	
Attributes, Netlist Screener. (Text Book 1: Chapter 9: 9.1 to 9.1.11)	
ASIC Construction: Physical Design, CAD Tools, System partitioning,	
Estimating ASIC size, Constructive Partitioning, Iterative Partitioning	
Improvement, KL Algorithm, FM and Look Ahead algorithms.	
(Text Book 1: Chapter 15: 15.1, 15.2, 15.3, 15.4, 15.7.3, 15.7.4, 15.7.5,	
15.7.7)	
Module-4	8 Hours
Floor planning: Goals and objectives, Measurement of delay in Floor	L2, L3
planning, Floor planning tools, Channel definition, I/O and Power	
planning and Clock planning.	
Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative	
Placement Improvement, Physical Design Flow.	
(Text Book 1: Chapter 16: 16.1, 16.2.2, 16.2.4, 16.2.6, 16.3)	

Module-5	8 Hours
Routing: Global Routing: Goals and objectives, Global Routing Methods,	L2, L3
Global routing between blocks, Back-annotation. Detailed Routing: Goals	
and objectives, Measurement of Channel Density, Left-Edge Algorithm,	
Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed	
routing, Final routing steps.	
(Text Book 1: Chapter 17: 17.1.1, 17.1.3, 17.1.4, 17.1.7, 17.2.1, 17.2.2,	
17.2.4, 17.2.6, 17.2.7, 17.2.8, 17.2.9)	

CO1	Describe application specific integrated circuits and its types.
CO2	Analyze various programmable ASIC logic cells and I/O cells.
CO3	Understand steps involved in Low-Level Design Entry and construction of ASIC using CAD tools.
CO4	Implement Floor planning and Placement Algorithms.
CO5	Apply various routing algorithms used in physical design.

Textbooks:

Michael John Sebastian Smith Addison, Application - Specific Integrated Circuits, - Wesley Professional 2005.

Reference Books:

- 1. Adel Sedra and K. C. Smith, Microelectronics Circuits Theory and Applications, 7th Edition, Oxford University Press, International Version, 2009.
- 2. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Education (India) Private Limited, 2007.
- 3. Sung Mo Kang and Yosuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3rd Edition, McGraw Hill Education (India) Private Limited.

MOOCs:

https://www.youtube.com/watch?v=sV2xT-WCSSI https://www.youtube.com/watch?v=faiEVOOCe-s https://www.youtube.com/watch?v=arut8G4Ego0 https://www.youtube.com/watch?v=yyliRphXLq4 https://www.youtube.com/watch?v=egfHY-NOt6Y

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1.



Table 1: Distribution of weightage for CIE & SEE of Regular courses

	0 0		
	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	Ε0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50

	CO-PO and PSO Mapping													
CO/PO	PO1	P02	PO3	P04	P05	P06	P07	P08	P09	PO10	P011	PO12	PS01	PS02
CO1	3	3	3	-	1	-	1	-	-	-	-	2	2	2
CO2	3	3	3	-	1	-	-	-	-	-	2	2	2	2
CO3	3	3	3	-	1	-	-	1	-	1	2	2	2	2
CO4	3	3	3	-	1	-	-	1	-	1	2	2	2	2
CO5	3	3	3	-	1	-	1	-	-	-	2	2	2	2
Average	3	3	3	-	1	-	1	-	-	-	2	2	2	2

Low-1: Medium-2: High-3



SEMESTER –VIII Program Elective – 4

Course: Wireless Sensor Networks

Course Code	22ECE824	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students are taught;

	6 - 1
CLO1	Basic of Wireless Sensor Networks
CLO2	Fundamentals of MAC Layer protocols
CLO3	Routing Challenges and Design Issues in Wireless Sensor Networks
CLO4	Various Operating Systems for WSN.
CLO5	Applications of WSN

Introduction and Overview of Wireless Sensor Networks: Introduction, Background of Sensor Network Technology, Applications of Sensor Networks, Basic Overview of the Technology, Basic Sensor Network Architectural Elements. Basic Wireless Sensor Technology: Introduction, Sensor Node Technology,	ours .2
Background of Sensor Network Technology, Applications of Sensor Networks, Basic Overview of the Technology, Basic Sensor Network Architectural Elements. Basic Wireless Sensor Technology: Introduction, Sensor Node Technology,	.2
Networks, Basic Overview of the Technology, Basic Sensor Network Architectural Elements. Basic Wireless Sensor Technology: Introduction, Sensor Node Technology,	
Architectural Elements. Basic Wireless Sensor Technology: Introduction, Sensor Node Technology,	
Basic Wireless Sensor Technology: Introduction, Sensor Node Technology,	
Į į	
Hardware and Software, Sensor Taxonomy, WN Operating Environment.	
Wireless Transmission Technology and Systems: Introduction, Radio	
Technology Primer, Propagation and Propagation Impairments,	
Modulation, Available Wireless Technologies, Campus Applications,	
MAN/WAN Applications.(Text2: 1.1,1.2.1,3.1,3.2,3.3,3.4,4.1,4.2,4.3)	
Module-2 8 Ho	ours
Medium Access Control Protocols: Fundamentals of MAC protocols, Low	_3
duty cycle protocols and wakeup concepts, Contention based protocols.	
Schedule-based protocols: SMAC, BMAC ,Traffic-adaptive medium access	
protocol (TRAMA),The IEEE 802.15.4 MAC protocol.(Text1:	
5.1,5.2,5.3,5.4,5.5)	
Module-3 8 He	ours
Routing Protocols for WSN: Data Dissemination and Gathering, Routing L	_3
Challenges and Design Issues in Wireless Sensor Networks, Network Scale	
and Time-Varying Characteristics, Resource Constraints, Sensor	
Applications Data Model, Routing Strategies in Wireless Sensor Networks,	
WSN Routing Techniques, Flooding and Its Variants, Sensor Protocols for	
Information via Negotiation, Low-Energy Adaptive Clustering Hierarchy,	
Power-Efficient Gathering in Sensor Information Systems, Directed	
Diffusion, Geographical Routing.(Text2:6.1,6.2,6.3.6.4,6.5)	
Module-4 8 He	ours
	.3
systems, Programming paradigms and application programming interfaces,	.5
Structure of operating system and protocol stack Dynamic energy and	
power management, Examples of Operating Systems, TinyOS, Mate:	
MagnetOS, MANTIS, OSPM - EYES OS, SenOS, EMERALDS,	

PicOS: Introduction to Tiny OS, NesC: Interfaces and Modules,	
Configurations and Wiring, Generic Components, Programming in Tiny OS	
using NesC, Emulator TOSSIM.(Text1:2.3-2.3.1 to 2.3.4.	
Text2:10.1,10.2,10.3,10.4)	
Module-5	8 Hours
APPLICATIONS OF WSN Applications: Home Control, Building Automation,	L3
Industrial Automation, Medical Applications, Reconfigurable Sensor	
Networks, Highway Monitoring, Military Applications, Civil and	
Environmental Engineering Applications, Wildfire Instrumentation, Habitat	
Monitoring, Nanoscopic Sensor Applications. (Text 2: 2.3,2.4,2.5,2.6)	

CO1	Comprehend the basics, characteristics and challenges of Wireless Sensor Network
CO2	Apply appropriate physical and MAC layer protocols to design a WSN.
CO3	Identify the suitable routing algorithm based on the network and user requirement.
CO4	Describe the OS used in Wireless Sensor Networks and build basic modules
CO5	Explain the applications of WSN in various fields

Textbook:

- 1. Holger Karl and Andreas Willig, Protocols and Architectures for Wireless Sensor Network, John Wiley & Sons, 2005.
- 2. Kazem Sohraby, Daniel Minoli and Taieb Znati, Wireless Sensor Networks Technology, Protocols, and Applications, John Wiley & Sons, 2007.

Reference Books:

- 1. K. Akkaya and M. Younis, A survey of routing protocols in wireless sensor networks, Elsevier Ad Hoc Network Journal, Vol. 3, no. 3, pp. 325—349.
- 2. Anna Hac, Wireless Sensor Network Designs, John Wiley & Sons Ltd.

e- Books:

https://digitalforensicforest.com/wp-content/uploads/2017/10/WSN-kazem-sohraby.pdf

MOOCs:

https://nptel.ac.in/courses/106105160

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1.



Table 1: Distribution of weightage for CIE & SEE of Regular courses.

	Component	Marks	Total
	Component	IVIAIKS	
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	50
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50

					CO-PC	and I	PSO M	appin	g					
CO/PO	P01	P02	P03	P04	P05	P06	P07	P08	P09	PO10	P011	PO12	PS01	PS02
CO1	2					1							2	2
CO2	1	2		2									1	1
CO3	2												1	1
CO4										2		2	1	1
CO5													2	2
Average	2	2		2		1				2		2	2	2

Low-1: Medium-2: High-3



SEMESTER -VIII Program Elective - 5

Course: Internet of Things and Cloud Computing

Course Code	22ECE831	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

CLO1	IoT and its deployment
CLO2	M2M and IoT system Management
CLO3	IoT Platforms and design Methodology
CLO4	Cloud computing and Virtualization
CLO5	Role of cloud computing in IoT.

Content	No. of Hours / RBT levels
Module-1	8 Hours
Introduction to Internet of Things: Introduction, Physical Design of IoT,	L2
Logic Design of IoT, IoT Enabling Technologies, IoT Levels & Deployment	
Templates. Domain Specific IoTs- Home Automation, Environment (Text-	
1: 1.1, 1.2, 1.3, 1.4, 1.5, 2.1 & 2.4)	
Module-2	8 Hours
M2M and IoT System Management: Difference between IoT and M2M , SDN and NFV for IoT	L2
IoT System Management with NETCONF-YANG: Need for IoT Systems	
Management, Simple Network Management Protocol (SNMP), Network	
Operator Requirements, NETCONF, YANG, IoT Systems Management with	
NETCONF-YANG (Text-1: 3.2, 3.3, 3.4.1, 4.2, 4.3, 4.4, 4.5 & 4.6)	
Module-3	8 Hours
IoT Platforms and Design Methodology: IoT Design Methodology, Case	L3
Study on IoT System for Weather Monitoring, What is an IoT device,	
Exemplary device Raspberry Pi, About the board , Interfaces,	
Programming Raspberry pi with Python (Text1 :5.2, 5.3, 7.1, 7.3, 7.5 & 7.6)	
Module-4	8 Hours
Introduction to Cloud and Virtualization: Introduction ,Cloud Computing at a Glance, The Vision of Cloud Computing, Defining a Cloud, A Closer Look, Cloud Computing Reference Model, Characteristics and Benefits, Challenges Ahead, Virtualization, Introduction, Characteristics of	L3
Virtualized, Environments Taxonomy of Virtualization Techniques, Execution Virtualization, Other Types of Virtualization, Virtualization and	
Cloud Computing, Pros and Cons of Virtualization, Technology Examples Xen: Paravirtualization, VMware: Full Virtualization, Microsoft —Hyper V	
(Text2: 1.1, chapter 3)	_
Module-5	8 Hours
Cloud Computing Architecture: Cloud Computing Architecture,	L3
Introduction, Cloud Reference Model, Architecture, Infrastructure /	
Hardware as a Service, Platform as a Service, Software as a Service, Types	
of Clouds, Public Clouds, Private Clouds, Hybrid Clouds, Community	
Clouds, Economics of the Cloud, Open Challenges, Cloud Definition, Cloud	

Interoperability and Standards Scalability and Fault Tolerance Security,	
Trust, and Privacy Organizational Aspects (Text2 : chapter 4)	

CO1	Explain the various concept of the IoT and their technologies.
CO2	Discuss IoT system management through SNMP protocol
CO3	Apply IoT design methodology to develop simple programs using Raspberry pi
	board.
CO4	Explain cloud computing and Architecture.
CO5	Describe the Architectures, services and models of the cloud.

Textbooks:

- 1. Bahga, Arshdeep., Madisetti, Vijay. Internet of Things: A Hands-on Approach. United Kingdom: Arshdeep Bahga & Vijay Madisetti, 2014.
- 2. Rajkumar Buyya, Christian Vecchiola, and Thamarai Selvi Mastering Cloud. Computing McGraw Hill Education, 2013

Reference Books:

1. Jayaswal, Kallakurchi, Houde, Shah, KLSI, Cloud Computing Black Book,, Dreamtech Press, 2012

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses.

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50



					CC)-PO a	nd PSC) Мар	ping					
СО	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	1	2	-	-	-	-	-	-	-	-	1	-	2
CO2	-	-	3	2	2	-	-	-	-	-	-	2	1	3
CO3	-	-	-	-	-	-	-	-	-	-	-	1	1	1
CO4	-	-	3	-	-	-	-	-	-	-	-	2	1	1
CO5	-	-	2	2	3	-	-	-	-	-	-	2	1	3
Average	•	1	3	2	3	-	-		-	-	ı	2	1	2

Low-1: Medium-2: High-3



SEMESTER – VIII Program Elective – 5

Course: High-Performance Computer Networks

Course Code	22ECE832	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Computer Communication Networks

Course Learning Objectives: Students will be taught;

CLO1	Communication Networks, Network Services, and layered Architecture
CLO2	Different Internet protocols
CLO3	Circuit-Switched Networks and Wireless Networks

Content	No. of Hours/
Madula 1	RBT levels
Module 1	8 Hours
History of Communication Networks: History of Communication Networks,	L2
Networking principles, Future Networks Internet, Pure ATM Network, Cable	
Network, Wireless. (Text-1,1.1 to 1.3.4)	
Module 2	8 Hours
Network Services and Layered Architectures: Applications, Traffic	L2
characterization and quality of service, Network services, High-Performance	
networks, Network Elements, Basic Network Mechanisms, Layered	
Architecture, Open data network model, Network architectures, Network	
bottlenecks. (Text-1,2.1 to 2.10)	
Module 3	8 Hours
The Internet and TCP/IP Networks: The Internet, Overview of Internet	L3
Protocols, Internet Protocol, TCP and UDP, Internet success and limitation,	
Performance of TCP/IP Networks. (Text-1,4.1 to 4.6)	
Module 4	8 Hours
Circuit Switched Networks: Performance of Circuit-Switched Networks,	L2
SONET, Dense Wave-Division Multiplexing (DWDM), Fiber to the Home,	
Digital Subscriber Line (DSL), Intelligent Networks, CATV (Text-1, 5.1 to 5.7)	
Module 5	8 Hours
Wireless Networks: The Wireless Channel, Link Level Design, Channel	L3
Access, Network Design, Wireless Networks Today, Future Systems and	
Standards. (Text-1, 7.2 to 7.7)	

Course Outcomes: Upon completion of this course, student will be able to:

CO1	Understand the communication network principles and future networks.
CO2	Understand the network services and layered architectures.
CO3	Explain the Internet and different protocols.
CO4	Understand the performance of circuit-switched networks
CO5	Explain the design principle and channel access for wireless Networks

Textbooks:

1. Jean Warland, Pravin Varaiya: Morgan "High-Performance Communication Networks", Kauffman/Elsevier 2nd Edition Kauffmann Publishers 2000

Reference Books:

- 1. William Stallings "High-Speed Networks and Internet: Performance and Quality of Service" Pearson Edu., 2001.
- 2. James F.Kurose, Keith W.Ross "Computer Networks", ,2nd Edition, Pearson Education 2003

MOOCs:

https://onlinecourses.nptel.ac.in/noc23_cs35/preview https://www.coursera.org/learn/computer-networking https://onlinecourses.nptel.ac.in/noc22_cs19/preview

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
CO/PO	PO1	P02	PO3	PO4	PO5	P06	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PS02
CO1	3	2	1	-	-	-	-	-	-	-	-	-	1	2
CO2	3	2	2	-	-	-	-	-	-	-	-	-	1	2
CO3	3	2	2	-	-	-	-	-	-	-	-	-	1	2
CO4	3	2	2			-	-	-	-	-	-		1	2
CO5	2	2	2			-	-	-	-	-	-		1	2
Average	2	2	2			-	_	-	_	-	-		1	2

Low-1: Medium-2: High-3

SEMESTER – VIII Program Elective – 5

COURSE: Multimedia Communication

Course Code	22ECE833	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Prerequisites: Computer Communication Networks

Course Objectives: Students will be taught;

CLO1	Fundamentals of Multimedia Communication and different multimedia networks
	and applications.
CLO2	Digitization principle techniques required to analyze different media types.
CLO3	Text and Image Compression techniques and gain knowledge of DMS.
CLO4	Audio and Video compression techniques.
CLO5	Gain fundamental knowledge about multimedia communication across different
	networks.

Content	No. of Hours/ RBT levels
Module 1	8 Hours
Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications and networking terminology. (Text 1)	L2
Module 2	8 Hours
Information Representation : Introduction, Digitization principles, Text, Images, Audio and Video. (Text 1)	L2
Module 3	8 Hours
Text and image compression: Introduction, Compression principles, text compression, image Compression. (Text 1) Distributed multimedia systems: Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia operating systems (Text 2).	L2
Module 4	8 Hours
Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Text 1).	L2
Module 5	8 Hours
Multimedia Communication Across Networks: Packet audio/video in the network environment, Video transport across generic networks, Multimedia Transport across ATM Networks. (Text 2).	L2

COURSE OUTCOMES: Upon completion of this course, student will be able to;

CO1	Explain the basic of different multimedia networks & applications.
CO2	Analyze different media types to represent them in digital form.
CO3	Compare different types of text and images using different compression techniques
CO4	Explain the different types of compression techniques to compress audio and video.
CO5	Describe multimedia Communication across Networks.

Text books:

- 1. Fred Halsall, Multimedia Communications: Applications, Networks, Protocols and Standards, 1st Edition, Pearson education, 2001.
- 2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, Multimedia Communication Systems, 1st Edition, Pearson education, 2004.

Reference book:

1. Raifsteinmetz, Klara Nahrstedt, Multimedia: Computing, Communications and Applications, 1st Edition, Pearson education, 2002.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any five full questions choosing at least one full question from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total Marks
	CIE Test-1	40	50
CIE	CIE Test-2	40	50
	CIE Test-3	40	
	Assignments	10	
SEE	Semester End Examination	50	50
	100		



					C	О-РО	and PS	O Ma _l	ping					
СО	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	1	-	1	-	-
CO2	3	2	_	-	-	-	-	-	-	1	-	1	-	-
CO3	3	2	-	-	-	-	-	-	-	1	-	1	-	-
CO4	3	2	-	-	-	-	-	-	_	1	-	1	-	-
CO5	3	2	-	-	-	-	-	-	-	1	-	1	-	-
Aver age	3	2	-	-	-	-	-	-	-	1	-	1	-	-

Low-1: Medium-2: High-3

SEMESTER – VIII Program Elective – 5

Course: Digital Switching Systems

Course Code	22ECE834	CIE Marks	50
Hours/Week (L: T: P)	3:0:0	SEE Marks	50
No. of Credits	3	Examination Hours	03

Course Learning Objectives: Students will be taught;

	<u> </u>
CLO1	Basics of telecommunication networks and digital transmission of data.
CLO2	Evolution of switching systems and the digital switching.
CLO3	Telecommunication traffic and its measurements.
CLO4	Technologies associated with the data switching operations.
CLO5	Hardware and software architecture of Digital Switching Systems.

services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH. (Text 1: 1.1 to 1.6 and 2.1 to 2.7) Module-2	Content	No. of Hours / RBT levels
services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH. (Text 1: 1.1 to 1.6 and 2.1 to 2.7) Module-2	Module-1	8 Hours
telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH. (Text 1: 1.1 to 1.6 and 2.1 to 2.7) Module-2 Evolution of switching systems: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution frames, Electronic switching, Introduction, Digital Switching System Analysis, Basic Central Office Linkages, switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Digital Switching System Fundamentals, Building blocks of a digital switching system, Basic call processing. (Text 2: 1.1 to 1.4) Module-3 Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	Development of telecommunications: Network structure, Network	L2
transmission, FDM, TDM, PDH and SDH. (Text 1: 1.1 to 1.6 and 2.1 to 2.7) Module-2 Evolution of switching systems: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution frames, Electronic switching. (Text 1: 3.1 to 3.3 3.5, 3.8, 3.11) Switching system fundamentals: Introduction, Digital Switching System Analysis, Basic Central Office Linkages, switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Digital Switching System Fundamentals, Building blocks of a digital switching system, Basic call processing. (Text 2: 1.1 to 1.4) Module-3 Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching Systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	services, terminology, Regulation, Standards. Introduction to	
Evolution of switching systems: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution frames, Electronic switching. (Text 1: 3.1 to 3.3 3.5, 3.8, 3.11) Switching system fundamentals: Introduction, Digital Switching System Analysis, Basic Central Office Linkages, switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Digital Switching System Fundamentals, Building blocks of a digital switching system, Basic call processing. (Text 2: 1.1 to 1.4) Module-3 Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	telecommunications transmission, Power levels, Four wire circuits, Digital	
Evolution of switching systems: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution frames, Electronic switching. (Text 1: 3.1 to 3.3 3.5, 3.8, 3.11) Switching system fundamentals: Introduction, Digital Switching System Analysis, Basic Central Office Linkages, switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Digital Switching System Fundamentals, Building blocks of a digital switching system, Basic call processing. (Text 2: 1.1 to 1.4) Module-3 Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	transmission, FDM, TDM, PDH and SDH. (Text 1: 1.1 to 1.6 and 2.1 to 2.7)	
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Switching system fundamentals: Introduction, Digital Switching System Analysis, Basic Central Office Linkages, switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Digital Switching System Fundamentals, Building blocks of a digital switching system, Basic call processing. (Text 2: 1.1 to 1.4) Module-3 Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	switching, Functions of switching systems, Distribution frames, Electronic switching. (Text 1: 3.1 to 3.3 3.5, 3.8, 3.11)	
Evolution of digital switching systems, Stored program control switching systems, Digital Switching System Fundamentals, Building blocks of a digital switching system, Basic call processing. (Text 2: 1.1 to 1.4) Module-3 Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	Switching system fundamentals: Introduction, Digital Switching System	
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Module-3 Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	Evolution of digital switching systems, Stored program control switching	
Module-3 Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	systems, Digital Switching System Fundamentals, Building blocks of a	
Telecommunication Traffic: Introduction, the unit of Traffic, Congestion, Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	digital switching system, Basic call processing. (Text 2: 1.1 to 1.4)	
Traffic measurement, a mathematical model, lost call systems, Queuing systems. (Text 1: 4.1 to 4.7) Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	Module-3	8 Hours
Module-4 Switching System Software: Introduction, Scope, Basic Software Architecture, Call Models, Software Linkages during a Call, Call Features (Text 2: 5.1 to 5.6). Maintenance of Digital Switching Systems: Software Maintenance, Interfaces of a Typical Digital Switching Central office, A methodology for Reporting and correction of Field Problems, Diagnostic Capabilities for proper maintenance on Digital Switching systems. (Text 2: 7.3, 7.4, 7.8 and 7.9). Module-5 A Generic Digital Switching System Model: Introduction, Scope, Hardware Architecture, Software Architecture, Recovery Strategy, A simple Call Through a Digital Switching System, Some common characteristics of Digital Switching Systems, Analysis Report. (Text 2: 9.1 to	Telecommunication Traffic: Introduction, the unit of Traffic, Congestion,	L3
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CO1	Describe the electromechanical switching systems and its comparison with the
	digital switching.
CO2	Describe the building blocks of digital switching systems and its functions.
CO3	Determine the telecommunication traffic and its measurements.
CO4	Explain Digital Switching software and its maintenance.
CO5	Elaborate the functions of A Generic Digital Switching Systems Model.

Textbooks:

- 1. J E Flood, Telecommunications Switching, Traffic and Networks, 22nd impression, Pearson Education Ltd, 2016.
- 2. Syed R. Ali, Digital Switching Systems, McGraw Hill Education (india) Private Limited, 16th reprint, 2018.

Reference Book:

1. John C Bellamy, Digital Telephony: Wiley India Pvt. Ltd, 3rd Edition, 2008.

Scheme of Examination:

Semester End Examination (SEE):

SEE Question paper is to be set for 100 marks and the marks scored will be proportionately reduced to 50. There will be two full questions (with a maximum of three sub questions) from each module carrying 20 marks each. Students are required to answer any **five full questions** choosing at least **one full question** from each module.

Continuous Internal Evaluation (CIE):

Three Tests are to be conducted for 40 marks each. Average of Marks scored in all three tests is added to test component. CIE is executed by way of quizzes / Alternate Assessment Tools (AATs), and three tests. Some possible AATs: Seminar/assignments/ mini-projects/ concept videos/ partial reproduction of research work/ group activity/ any other. Typical Evaluation pattern for regular courses is shown in Table 1

Table 1: Distribution of weightage for CIE & SEE of Regular courses

	Component	Marks	Total
			Marks
	CIE Test-1	40	
CIE	CIE Test-2	40	F0
CIE	CIE Test-3	40	50
	Assignments	10	
SEE	Semester End Examination	50	50
	100		

	CO-PO and PSO Mapping													
CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	-	-	-	-	-	-	-	-	-	-	1	-
CO2	1	1	1	-	-	-	-	-	-	-	-	-	1	1
CO3	1	2	-	-	-	-	-	-	-	-	-	1	1	-
CO4	3	3	2	-	-	-	-	1	-	-	-	1	2	1
CO5	2	1	_	-	_	_	_	1	_	-	-	1	2	1
Average	2	2	-	-	_	-	-	1	-	-	-	1	2	1

Low-1: Medium-2: High-3

SEMESTER - VIII

Course: Project Work Phase-II

Course Code	22ECEP84	CIE Marks	100
Hours/Week (L: T: P)	2 hr/week	SEE Marks	100
No. of Credits	8	Examination Hours	3

CIE procedure for Project Work Phase - II:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -II, shall be based on the evaluation of the project work phase -II Report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the Project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -II, shall be based on the evaluation of the project work phase -II Report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the Project report shall be the same for all the batch mates.

SEE for Project Work Phase - II:

- (i) Single discipline: Contribution to the project and the performance of each group shall be assessed individually in semester end examination (SEE) conducted at the department.
- (ii) Interdisciplinary: Contribution to the project and the performance of each group shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belongs to.



SEMESTER - VIII

Course: Technical Seminar

Course Code	22ECES85	CIE Marks	100
Hours/Week (L: T: P)	One hour/week	SEE Marks	-
No. of Credits	1	Examination Hours	-

The CIE marks awarded for Technical Seminar shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

SEMESTER - VIII

Course: Internship

Course Code	22INT86	CIE Marks	100
Hours/Week (L: T: P)		SEE Marks	-
No. of Credits	2	Examination Hours	-

All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared fail and shall have to complete during subsequent examination after satisfying the internship requirements.

Department of Electronics and Communication Engg. Global Academy of Technology Bengaluru-98 Clarel Academy of Technology,